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## Research Paper

# Controlling Ambipolar Current in a Junctionless Tunneling FET Emphasizing on Depletion Region Extension

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**Keywords:**
**Junctionless tunneling field effect transistors (J-TFETs); Band-to-band tunneling (BTBT); Ambipolar current; Depletion region; Tunneling barrier width.**

## Abstract:

For the first time, in this research, we introduce a junctionless tunneling FET (J-TFET) on a uniform $p^+$ starting junctionless FET to realize appreciable immunity against inherent high ambipolar current ($I_{amb}$). So, we utilize two isolated gates with appropriate workfunctions over the channel and drain regions to create $P^+IP^+N^+$ charge distribution. This structure utilizes a space between the gate-drain electrodes ($S_{GD}$), to provide a $P^+IP^+N^+$ structure thanks to the effective electrons depletion on the drain side. Increasing the $S_{GD}$, further effectively pulls up the bands near the interface between the channel-drain regions, widens the tunneling width for tunneling to occur, and thus in turn reduces the $I_{amb}$ from $5.37\times10^{-7}$ A/μm to $1.14\times10^{-14}$ A/μm. Thus, we point out that the proposed J-TFET can obtain on-current that satisfies the expectation of logic applications with high performance and $I_{off}$ that meets the specifications of low power characteristics, a phenomenon that is rarely accessible with conventional TFETs.

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## 1. INTRODUCTION

MOSFETs are continuing to scale down and thus their power consumption is becoming an important concern. Lowering the standby power ($I_{off} \times V_{DD}$) is crucial, ($I_{off}$ being the leakage current; and $V_{DD}$ the supply voltage) in low power applications [1-3]. Thus reducing $I_{off}$ and scaling down $V_{DD}$ are the momentous schemes employed in low power design of MOSETs, which means the steep subthreshold slope in the devices [4-8]. However, a limit of 60 mV/decade for the subthreshold swing (*SS*) is quite well known in MOSFETs [4-8]. This limit of subthreshold swing which stems from the thermal injection of current carriers over the source channel energy barrier is unfortunately no longer sufficient to ensure high on/off current ratio ($I_{on}/I_{off}$) when low $V_{DD}$ is desired. Due to this limitation, there is a renewed and growing interest in exploring a replacement for MOSFET, a device which can potentially provide higher $I_{on}/I_{off}$ for a given supply voltage.

In particular, there is a strong push towards devices which utilize band alignment along with the band to band tunneling (BTBT) mechanism. These devices have the opportunity to provide noticeable low $I_{off}$ and promise the potential of obtaining *SS* values below the 60 mV/dec theoretical limit seen in the MOSFETs. From this point of view, Tunneling Field Effect Transistor (TFET) has been the subject of intense investigations in recent years. Since in this type of device, the current depends on the BTBT mechanism rather than thermal injection over the barrier [4-8].

However, TFET suffers from three major shortcomings. These are (1) an unacceptably low $I_{on}$ [9-25]; (2) ambipolar current ($I_{amb}$), a unique conduction property seen for high negative gate voltage, which limits application of transistor in low-power circuit design [24-33]; (3) use of abrupt high doped junctions needed for efficient tunneling. Fabrication of such junctions of course requires complex high thermal budget processes and yet hard to obtain because of the doping diffusion [34-36]. It is then natural to exercise attempts to improve both TFET performance and its device manufacturability.

So far, several novel structure have been introduced to enhance the $I_{on}$ [9-25], while only a modest efforts have been devoted to the improve on the $I_{amb}$ and abrupt high doped junction requirements [24-33, 37-39].

A novel structure called junctionless tunneling FET (J-TFET) has recently been introduced which has very simple structure and thus amenable to manufacturing [37-39]. It is in fact a tunnel FET without any sharp doping profiles. The J-TFET offers superior performance since it blends the advantages of both JN-FET [40-46] and TFET [4-8] structures. Although, the newly proposed J-TFET overcomes the challenges of low $I_{on}$, high *SS* values, and also abrupt high doped junctions, it still suffers from a detrimental problem i.e. high $I_{amb}$ [37-38].

In this study, we will introduce a technique to achieve a J-TFET with $P^+IN^+$ charge distribution. This structure acts similar to the conventional TFET (C-TFET). For the first time, as the proposed J-TFET is fabricated on a junctionless $P^+$ starting substrate (PJ-TFET), it needs no metallurgical junctions and thus it is free from random dopant fluctuations. Also for suppression of inherent ambipolar conductivity, the electrons of the drain side are extremely depleted to realize a $P^+IP^+N^+$ charge distribution. This leads to tunneling width extension near the interface of channel-drain, negligible electrons tunneling from channel region into the drain end and thus suppression of $I_{amb}$ as discussed below.

## 2. DEVICE PARAMETERS AND SIMULATION MODELS

To investigate the electrical characteristics of the proposed PJ-TFET, we will evaluate it by a 2D device simulator employing Silvaco Atlas [47]. The cross-sectional views of the junctionless FET (J-FET) and PJ-TFET are exhibited in Fig. 1(a) and Fig. 1(b), respectively. The PJ-TFET structure is a lateral p-type J-FET, which uses two isolated gates called the Main-Gate (MG) and the N-Gate (NG), each with appropriate work-functions, to make the silicon thin film beneath the channel and drain regions intrinsic and n-type, respectively. Thus, the main idea here is to convert the ($P^+$-$P^+$-$P^+$) source, channel and drain of the J-FET with doping concentration of $1\times10^{19}$ $cm^{-3}$ into a ($P^+$-I-$N^+$) structure without any use of physical doping. While the MG is responsible for turning the device into the on state, the NG is kept at zero voltage in both the off and the on states. Employing the NG creates a space between the gate-drain electrodes ($S_{GD}$), which manages the tunneling barrier width near the drain side as well as reduces the $I_{amb}$. The parameters utilized for the two structure in our study are listed in Table I.

To consider lateral direction for the tunneling, we have used nonlocal BTBT model in the simulation [16-17, 29, 34]. The nonlocal BTBT model can describe carrier transport along the barrier with assuming entire tunneling path. Thermal generation-recombination is a major motivation for employing the Shockley-Read-Hall (SRH) model. Also direct recombination (Auger) [41] and band gap narrowing (BGN) models are taken into account because of the high doping concentration in the junctionless device structure. The doping-dependent and field-dependent mobility degradations were considered by employing the Philips as well as Lombardi mobility models, respectively. Although, the quantum phenomena are applied by Hänsch et al. [48], this can be neglected because the thickness of silicon film is above 7 nm [49, 50].

Calibration of simulation models against results obtained from an experimental TFET under similar conditions is shown in Fig. 2 [5]. It is clear from the figure how well simulation results are in close agreement versus experimental data. This indicates that the models used in this study truly capture the BTBT mechanism.

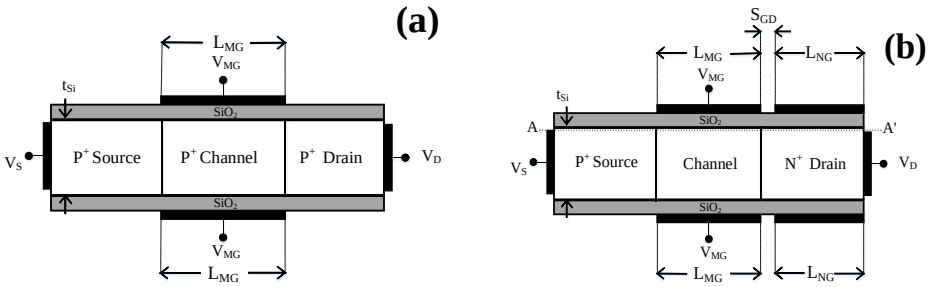


**Fig. 1**. Schematic of the (a) J-FET, and the (b) PJ-TFET structures.

## 3. RESULT AND DISCUSSION

### 3.1. DEVICE PHYSICS OF THE PJ-TFET

Fig. 3(a) exhibits band diagrams for the PJ-TFET structure in the off-states. It is observed that the probability of the electron tunneling is negligible since the barrier width near the source-channel interface is very large. Thus the carrier concentration under the MG is very small and the device behaves similar to a $P^+$-I-$N^+$ structure as illustrated in Fig. 3(b). Fig. 3(c) exhibits the band diagram in the on-state. Applying a positive gate voltage on the MG, turns the device on.

**Table. I. Parameters used for the devices simulation**

| Parameters | PJ-TFET | J-FET |
|---|---|---|
| Main-Gate (MG) length ($L_{MG}$) | 30 nm | 30 nm |
| N-Gate (NG) length ($L_{NG}$) | 29 nm | - |
| Space between the MG and NG ($S_{GD}$) | 1 nm | - |
| Silicon film thickness ($t_{si}$) | 10 nm | 10 nm |
| Gate oxide ($SiO_2$) thickness ($t_{ox}$) | 1 nm | 1 nm |
| MG's workfunction | 4.1 eV | 4.1 eV |
| NG's workfunction | 2.9 eV | - |

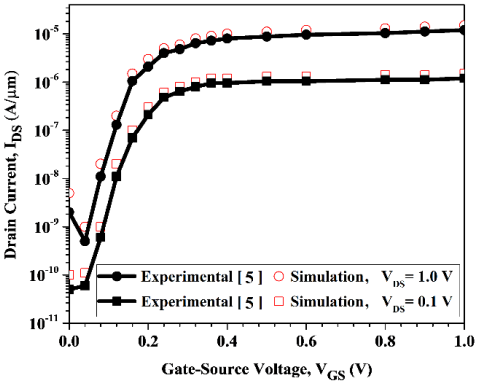


**Fig. 2**. Calibration of the transfer characteristics ($I_{DS}$-$V_{GS}$) against experimental results.

Under such biasing conditions, the barrier near the source-channel interface narrows down. Thus there is a high probability of electrons tunneling from source into the channel, which the conductivity in this region becomes almost n-type region as shown in Fig. 3(d). Note that due to proper choice of NG workfunction, the electron concentration in the drain region remains constant at about $N_D = 1\times10^{19}$ $cm^{-3}$. So the conductivity type has changed effectively from $p^+$ into an $n^+$. In all of these figures, the lateral direction is taken along the AA' cutline located at 0.1 nm under the $SiO_2$/Si interface. Fig. 4 also depicts the contour plots of the hole and electron concentrations in the off- and the on-states. It can be observe that for the PJ-TFET, either in the off-state or on-state conditions, the induced carrier concentrations are approximately comparable with that of the conventional TFET (C-TFET).

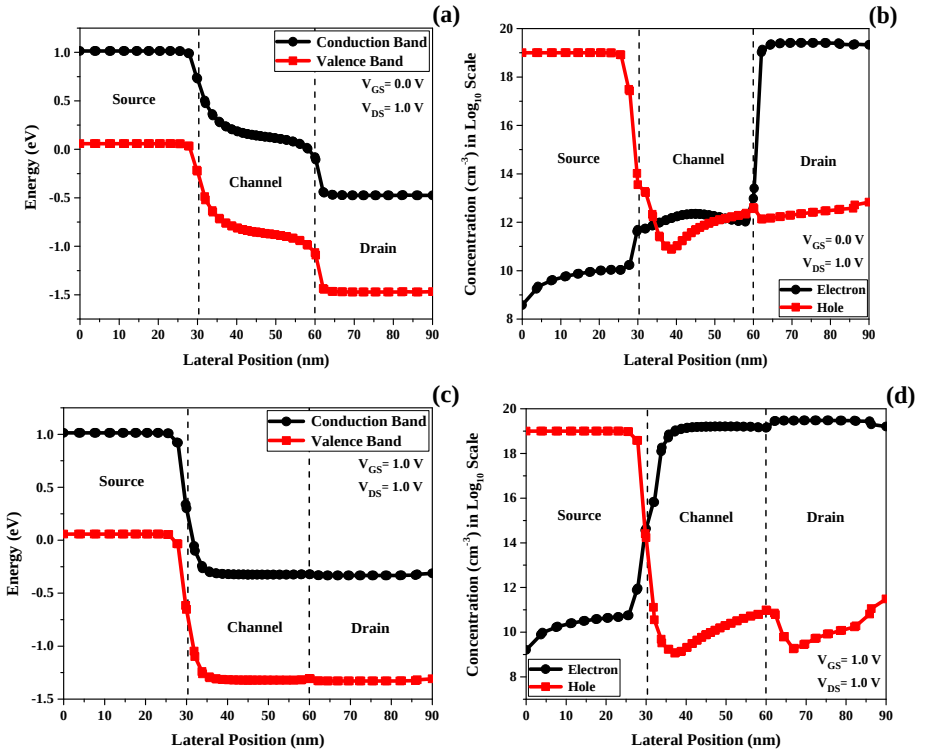


**Fig. 3.** (a) Band diagrams and (b) carrier concentrations of the PJ-TFET in the off-state. (c) Band diagrams and (d) carrier concentrations of the PJ-TFET in the On-state.

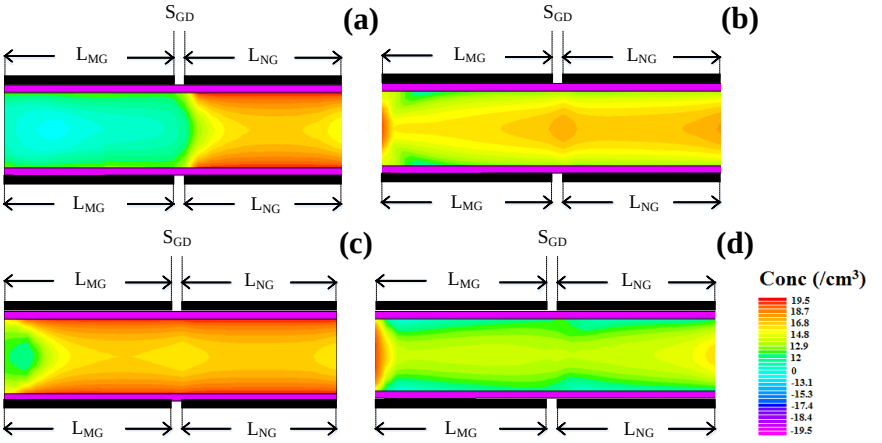


**Fig. 4.** Contour plots of the (a) electron and (b) hole concentrations in the off-state. (c) Electron and (d) hole concentrations in the on-state.

### 3.2. SUPPRESSION OF THE AMBIPOLAR CURRENT

In the PJ-TFET, the $I_{amb}$ is higher than the limit that can be tolerated for low power applications. In this section, we explain how the above structure can suppress the $I_{amb}$. The impact of the size of $S_{GD}$ on the PJ-TFET's transfer characteristics is shown in Fig. 5(a). A significant reduction in $I_{amb}$ is observed when the $S_{GD}$ is increased. Larger $S_{GD}$ is responsible for further depletion at the drain end. It also helps pulling up the band energy near the channel-drain interface which results in negligible electrons tunneling from channel into the drain. Also, Fig. 5(b) exhibits the $I_{amb}$ extracted at $V_{GS}$= -1.0 V, as a function of the $S_{GD}$ and $V_{DS}$. Since, the $S_{GD}$ determines the width of the tunneling barrier width, $I_{amb}$ is noticeably reduced as the $S_{GD}$ is increased.

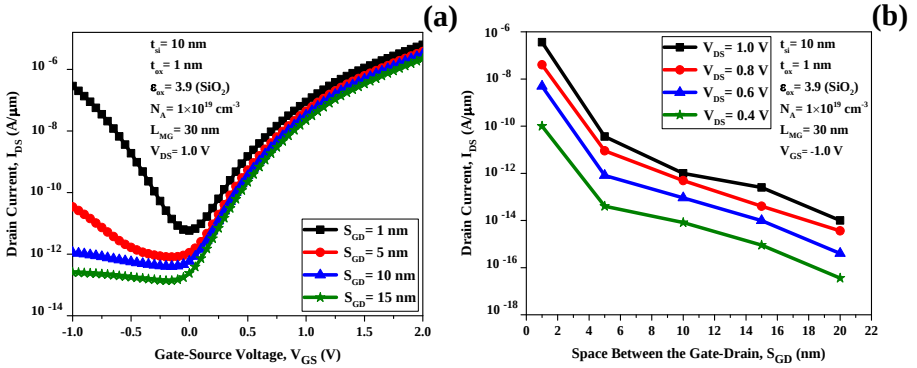


**Fig. 5.** (a) The PJ-TFET's transfer characteristics with spacing between the MG and NG as a parameter, (b) $I_{amb}$ as a function of $S_{GD}$ and $V_{DS}$ at $V_{GS}$= -1.0 V.

To see how $S_{GD}$ can affect the $I_{amb}$, refer to Fig. 6, where we have shown the band diagrams for the PJ-TFET in the lateral direction at $V_{GS}$= -1.0 V with $S_{GD}$ taken as parameter. To reduce the $I_{amb}$, the tunneling barrier width at the channel-drain interface should be large enough [18-24]. This can be achieved by increasing the $S_{GD}$. When $S_{GD}$ changes from 1 nm to 15 nm, the tunneling barrier width varies from 8 nm to 15 nm. Note that (due to employing of an auxiliary gate, NG, the drain voltage drops primarily on the gap between the MG and NG. This extends the off-state tunneling barrier into the drain region which in turn decreases the potential drop on this gap.

Fig. 7 demonstrates the electric field and BTBT rate for the PJ-TFET at

$V_{GS}$= -1.0 V with $S_{GD}$ taken as a parameter. It is clear that increasing $S_{GD}$, will reduce the maximum value of the electric field in the device and changes the position where electric field maximizes. The gap between the MG and NG is responsible for the penetration of the electric field into the drain, generating relatively small tunneling barrier width as shown in Fig. 6. Thus, for larger $S_{GD}$, the probability of electrons tunneling is negligible, leading to a small $I_{amb}$.

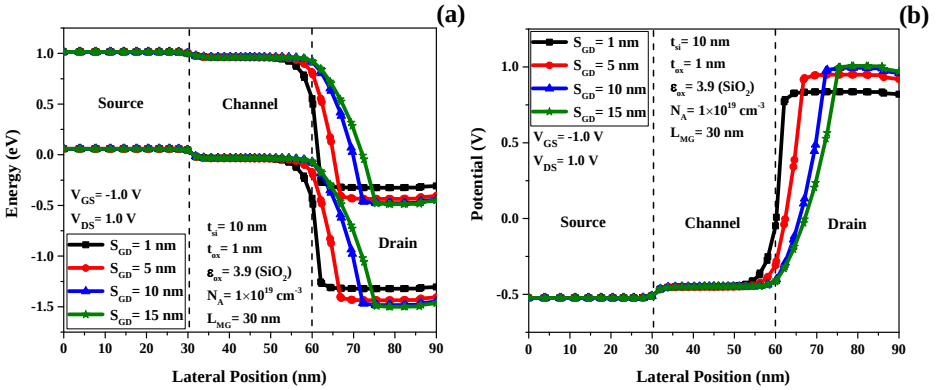


**Fig. 6.** The PJ-TFET's (a) band diagram and (b) potential along lateral direction for different values of the $S_{GD}$.

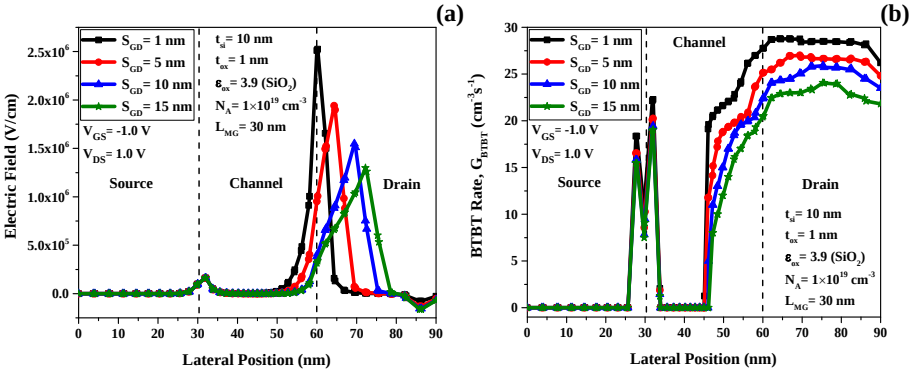


**Fig. 7.** (a) Electric field and (b) BTBT rate for different values of the $S_{GD}$ across lateral direction in the PJ-TFET.

Note that there are no electrically induced free carriers within the gap denoted by $S_{GD}$. This space is equivalent to the depletion region of electrons. Fig. 8 depicts the carrier concentrations across the PJ-TFET for different values

of $S_{GD}$. Larger $S_{GD}$ results in further depletion of electrons, which widens the tunneling width and hence significantly reduces the $I_{amb}$.

Also, Fig. 9 shows the contour plots of the electron concentrations for different values of $S_{GD}$ at $V_{GS}$= -1.0 V. As it is clear, the larger $S_{GD}$ facilitates depletion of electrons. Employing the NG realizes a novel design parameter, $S_{GD}$, to alleviate the $I_{amb}$. Therefore, this approach overcomes the main challenge of the $I_{amb}$ just by two electrodes on the channel and drain regions without any added structural sections which leads to a low thermal budget process.

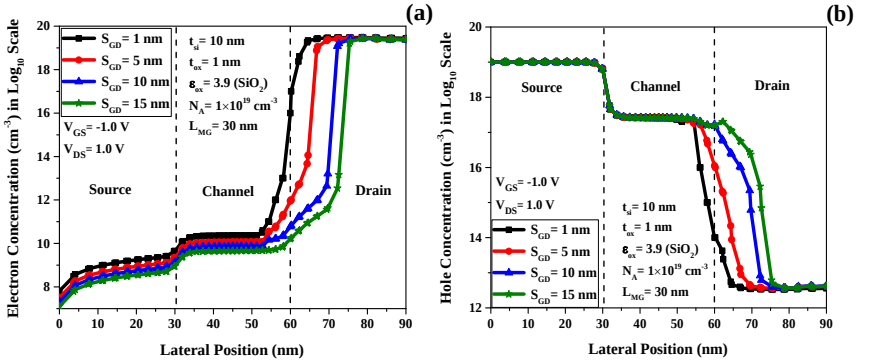


**Fig. 8.** (a) Electron and (b) hole concentrations along the lateral direction of the PJ-TFET when $S_{GD}$ increases from 1 nm to 15 nm.

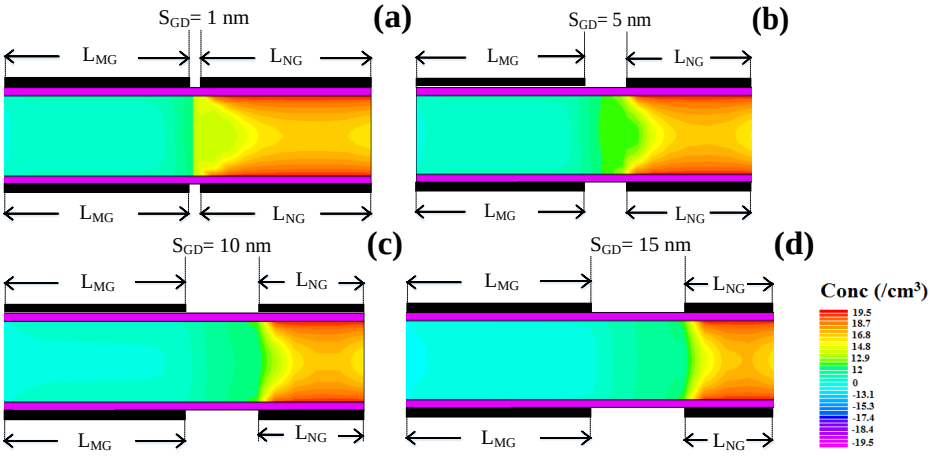


**Fig. 9.** Contour plots of electrons at $V_{GS}$= -1.0 V and $V_{DS}$= 1.0 V when $S_{GD}$ is equal to (a) 1 nm, (b) 5 nm, (c) 10 nm, (d) 15 nm.

### 3.3. DESIGN GUIDE LINES FOR THE PJ-TFET

Fig. 10(a) shows the PJ-TFET's transfer characteristics ($I_{DS}$-$V_{GS}$) for different values of $V_{DS}$. Observe that both the $I_{on}$ and $I_{off}$ increase when $V_{DS}$ is increased. Also, Fig. 10(b) compares the transfer characteristics, when metals with different workfunctions are employed for the NG. As implied by Fig. 10(b), choosing a higher workfunction of the NG, leads to pulling up the conduction as well as the valence band energies towards higher energies [16-17, 34]. In this fashion a considerably small band overlap between the channel and the drain region is achieved, which in turn reduces the tunneling efficiency and also $I_{amb}$.

Fig. 11 depicts the PJ-TFET's transfer characteristics for different thickness and different doping densities of the silicon film. Note also that $I_{off}$ is reduced when silicon film thicknesses is reduced [4-8]. Also, as shown in Fig. 11(b), $I_{on}$ increase with increase in the doping density of the silicon film [24]. Note that, when doping density is decreased, the $I_{off}$ is reduced without inflicting any noticeable change on the $I_{on}$. Employing lower doping density leads to further depletion of electrons near the drain side which is equivalent to extend the tunneling barrier width.

To study the impact of gate oxide thicknesses and dielectric constants, the transfer characteristics for the PJ-TFET are depicted in Fig. 12. From this figures, it is clear that a thinner gate oxide helps exerting a higher control on the channel potential [14, 19].

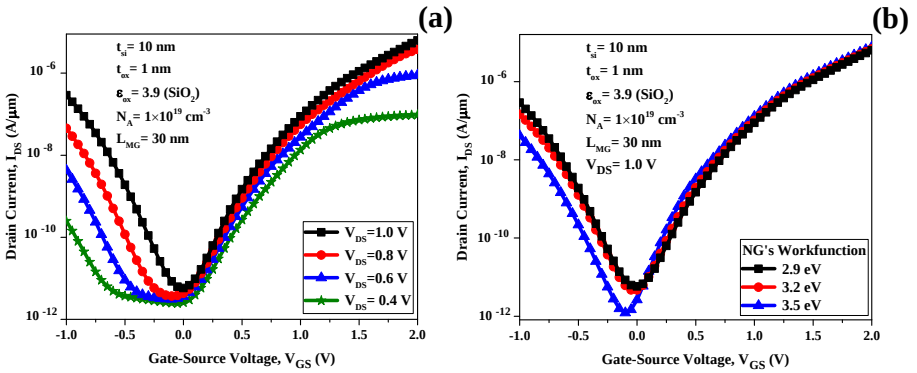


**Fig. 10.** The transfer characteristics when (a) $V_{DS}$ varies from 0.4 V to 1.0 V, (b) workfunction of the NG varies while workfunction of the MG is kept constant at 4.1 eV.

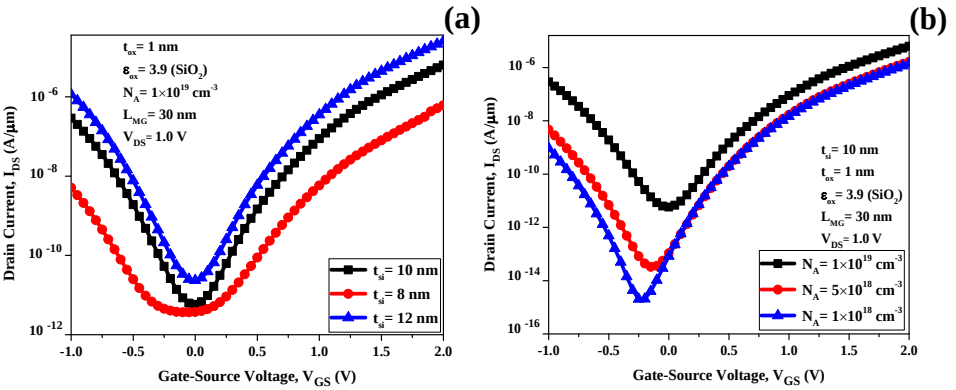


**Fig. 11.** The PJ-TFET's transfer characteristics with (a) silicon film thickness and (b) doping concentration of the silicon film chosen as parameter.

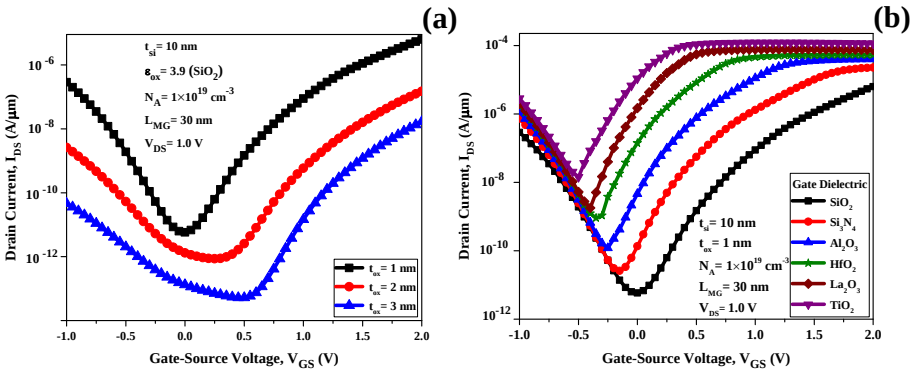


**Fig. 12.** The PJ-TFET's transfer characteristics with (a) thickness for the $SiO_2$ gate insulator and (b) gate oxide's dielectric constant as parameter.

Thus a thinner gate oxide leads to a larger $I_{on}$, while a thicker gate oxide provides a lower $I_{off}$. Also, a high $I_{on}$ can be achieved by a proper value of the gate dielectric [14, 19]. Here, different gate dielectrics are evaluated with $SiO_2$. As shown in Fig. 12 (b), in order to enhance the $I_{on}$, gate oxide's dielectric constant needs to be high. Therefore, lower thickness of the dielectric provides a solution for the low on-state current associated with the TFETs.

### 3.4. MODEL VALIDATION

In this part we will evaluate the proposed model in [51] for the PJ-TFET

structure by comparing it with the 2D TCAD simulation results. In [51], first we calculate the electric field and potential distribution by solving the 2-D Poisson's equation using Young's parabolic potential approximation. Next, an analytical drain current model is extracted by employing Kane's model which integrates the BTBT rate all over the tunneling region. We evaluate the efficacy of this model by varying some important parameters. **Fig. 13** demonstrates the PJ-TFET's transfer characteristics ($I_{DS}$-$V_{GS}$) with $S_{GD}$ as a parameter. As can be seen from the figure, the analytical model is tracking with good accuracy and closely approximates the simulation results.

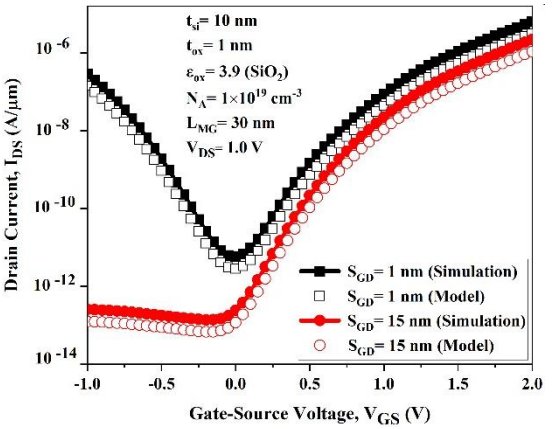


**Fig. 13.** The PJ-TFET's transfer characteristics ($I_{DS}$-$V_{GS}$) with $S_{GD}$ as a parameter for the proposed model (open symbols) and its comparison with simulation results (solid symbols).

## 4. CONCLUSION

In this paper, a new approach for realizing a J-TFET was proposed and a comprehensive investigation was carried out by using 2D device simulation. The proposed device structure provides a $P^+IN^+$ charge distribution and acts like a conventional TFETs. This approach utilizes an additional gate, here called N-Gate located apart from the Main-Gate, all on the $P^+$ starting junctionless FET. To further diminish the $I_{amb}$, we also proposed, a new structure which provides a $P^+IP^+N^+$ charge distribution obtained by the effective depletion of the electrons in the drain side. This leads to pulling the bands diagram up near the drain

region, causing insufficient band bending for tunneling to occur, and extending the tunneling barrier width at this region. Hence the $I_{amb}$ reduces.

## REFERENCES

[1] M. Rahimian and Ali. A. Orouji. *Investigation of the electrical and thermal performance of SOI MOSFETs with modified channel engineering*. Mater Sci Semicond Process., 16 (5) (Oct. 2013) 1248-1256. Available: https://doi.org/10.1016/j.mssp.2012.12.001

[2] M. Rahimian, Ali. A. Orouji and A. Aminbeidokhti. *A novel deep submicron SiGe-on-insulator (SGOI) MOSFET with modified channel band energy for electrical performance improvement*. Curr. Appl Phys., 13 (4) (Jun. 2013) 779-784. Available: https://doi.org/10.1016/j.cap.2012.12.005

[3] P. Bahrami, M. R. Shayesteh, M. Pourahmadi, H. Safdarkhani. *Improvement of the Drive Current in 5nm Bulk-FinFET Using Process and Device Simulations*. J Opt Nanostructures., 5 (1) (Feb. 2020) 65-81. Available: https://dorl.net/dor/20.1001.1.24237361.2020.5.1.5.0

[4] A. M. Ionescu and H. Riel. *Tunnel field-effect transistors as energy efficient electronic switches*. Nature., 479 (7373) (Nov. 2011) 329-337. Available: https://doi.org/10.1038/nature10679

[5] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu. *Tunneling Field-Effect Transistors (TFETs) with Subthreshold Swing (SS) Less Than 60 mV/dec*. IEEE Electron Device Lett., 28 (8) (Aug. 2007) 743–745. Available: https://doi.org/10.1109/LED.2007.901273

[6] Q. Zhang, W. Zhao and A. Seabaugh. *Low-Subthreshold-Swing Tunnel Transistors*. IEEE Electron Device Lett., 27 (4) (Apr. 2006) 297–300. Available: https://doi.org/10.1109/LED.2006.871855

[7] M. A. Eshkalak, R. Faez. *A Computational Study on the Performance of Graphene Nanoribbon Field Effect Transistor*. J Opt Nanostructures., 2 (3) (Aug. 2017) 1-12. Available: https://dorl.net/dor/20.1001.1.24237361.2017.2.3.1.9

[8] M. T. Björk, J. Knoch, H. Schmid, H. Riel, and W. Riess. *Silicon nanowire*

*tunneling field effect transistors*. Appl. Phys. Lett., 92 (Apr. 2008) 193504–193506. Available: https://doi.org/10.1063/1.2928227

[9] M. Rahimian and M. Fathipour. *Improvement of electrical performance in junctionless nanowire TFET using hetero-gate-dielectric*. Mater Sci Semicond Process., 63 (1) (Jun. 2017) 142–152. Available: https://doi.org/10.1016/j.mssp.2016.12.011

[10] D. Keighobadi, S. Mohammadi, M. Mohtaram. *Recessed Gate Cylindrical Heterostructure TFET, a Device with Extremely Steep Subthreshold Swing*. Trans. Electr. Electron. Mater., 23 (Apr. 2021) 81–87. Available: https://doi.org/10.1007/s42341-021-00321-4

[11] G. Musalgaonkar, Sh. Sahay, R. S. Saxena and M. J. Kumar. *Nanotube Tunneling FET With a Core Source for Ultrasteep Subthreshold Swing: A Simulation Study*. IEEE Trans. Electron Devices., 66 (10) (Oct. 2019) 4425–4432. Available: https://doi.org/10.1109/TED.2019.2933756

[12] M. Rahimian, and M. Fathipour. *Asymmetric junctionless nanowire TFET with built-in $n^+$ source pocket emphasizing on energy band modification*. J. Comput. Electron., 15 (4) (Dec. 2016) 1297–1307. Available: https://doi.org/10.1007/s10825-016-0895-1

[13] Z. Ahangari. *Switching Performance of Nanotube Core-Shell Heterojunction Electrically Doped Junctionless Tunnel Field Effect Transistor*. J Opt Nanostructures., 5 (2) (May. 2020) 1-12. Available: https://dorl.net/dor/20.1001.1.24237361.2020.5.2.1.8

[14] M. M. Ghiasvand, Z. Ahangari, H. Nematian. *Performance Optimization of an Electrostatically Doped Staggered Type Heterojunction Tunnel Field Effect Transistor with High Switching Speed and Improved Tunneling Rate*. J Opt Nanostructures., 7 (1) (Jan. 2022) 19-36. Available: https://doi.org/10.30495/jopn.2022.29617.1249

[15] M. K. Anvarifard, Ali A. Orouji. *Energy Band Adjustment in a Reliable Novel Charge Plasma SiGe Source TFET to Intensify the BTBT Rate*. IEEE Trans. Electron Devices., 68 (10) (Oct. 2021) 5284–5290. Available: https://doi.org/10.1109/TED.2021.3106891

[16] G. Musalgaonkar, Sh. Sahay, R. S. Saxena and M. J. Kumar. *A Line*

*Tunneling Field-Effect Transistor Based on Misaligned Core–Shell Gate Architecture in Emerging Nanotube FETs*. IEEE Trans. Electron Devices., 66 (6) (Jun. 2019) 2809–2816. Available: https://doi.org/10.1109/TED.2019.2910156

[17] A. N. Kumar, S. I. Amin, and S. Anand. *Design and Performance Optimization of Novel Core–Shell Dopingless GAA-Nanotube TFET With $Si_{0.5}Ge_{0.5}$-Based Source*. IEEE Trans. Electron Devices., 67 (3) (Mar. 2020) 789–795. Available: https://doi.org/10.1109/TED.2020.2965244

[18] M. Rahimian, and M. Fathipour. *Junctionless nanowire TFET with built-in n-p-n bipolar action: physics and operational principle*. J. Appl. Phys., 120 (22) (Nov. 2016) 225702. Available: https://doi.org/10.1063/1.4971345

[19] M. Roohy, R. Hosseini. *Performance Study and Analysis of Heterojunction Gate All Around Nanowire Tunneling Field Effect Transistor*. J Opt Nanostructures., 4 (2) (May. 2019) 13-28. Available: https://dorl.net/dor/20.1001.1.24237361.2019.4.2.2.2

[20] W. Li, H. Liu, Sh. Wang, Sh. Cheng, T. Han, K. Yang. *Design and investigation of dopingless dual-gate tunneling transistor based on line tunneling*. AIP Adv., 9 (Mar. 2019) 045109. Available: https://doi.org/10.1063/1.5087879

[21] R. M. Imen Abadi, S. Ali S. Ziabari. *Representation of strained gate-all-around junctionless tunneling nanowire filed effect transistor for analog applications*. Microelectron. Eng., 162 (16) (Aug. 2016) 12-16. Available: https://doi.org/10.1016/j.mee.2016.04.016

[22] I. Chahardah Cherik, S. Mohammadi. *Germanium‐source L‐shaped TFET with dual in‐line tunneling junction*. Appl. Phys. A., 127 (Jun. 2021) 525–532. Available: https://doi.org/10.1007/s00339-021-04677-5

[23] D. Shekhar, A. Raman. *Design and analysis of dual‐gate misalignment on the performance of dopingless tunnel field effect transistor*. Appl. Phys. A, 126 (May. 2020) 441–449. Available: https://doi.org/10.1007/s00339-020-03615-1

[24] A. K. Gupta, A. Raman, *Electrostatic-Doped Nanotube TFET: Proposal,*

*Design, and Investigation with Linearity Analysis.* Silicon, 13 (Jul. 2020) 2401–2413. Available: https://doi.org/10.1007/s12633-020-00584-1

[25] P. P. Goswami, B. Bhowmick, *Optimization of Electrical Parameters of Pocket Doped SOI TFET with L Shaped Gate*. Silicon, 12 (May. 2019) 693–700. Available: https://doi.org/10.1007/s12633-019-00169-7

[26] Sh. Sahay and M. J. Kumar, *Controlling the Drain Side Tunneling Width to Reduce Ambipolar Current in Tunnel FETs Using Heterodielectric BOX*. IEEE Trans. Electron Devices, 62 (11) (Nov. 2015) 3882–3886. Available: https://doi.org/10.1109/TED.2015.2478955

[27] D. B. Abdi and M. J. Kumar, *Controlling Ambipolar Current in Tunneling FETs Using Overlapping Gate-on-Drain*. IEEE J. Electron Devices Soc, 2 (6) (Nov. 2014) 187–190. Available: https://doi.org/10.1109/JEDS.2014.2327626

[28] M. Bavir, A. Abbasi, Ali. A. Orouji. *Dual $P^+$-Wire Double-Gate Junctionless MOSFET with 10-nm Regime for Low Power Applications*. J. Electron. Mater., 51 (Jan. 2022) 2083-2094. Available: https://doi.org/10.1007/s11664-022-09462-5

[29] D. Madadi, Ali. A. Orouji. *Stacked Single-Gate Silicon on Insulator 4H-SiC Junctionless Field-Effect Transistor with a Buried P-Type 4H-SiC Layer*. Phys. Status Solidi., 219 (11) (Jun. 2022) 2100504. Available: https://doi.org/10.1002/pssa.202100504

[30] M. Aslam, G. Korram, D. Sharma, Sh. Yadav, N. Sharma, *Enhancement of the DC performance of a PNPN hetero‐dielectric BOX tunnel field‐effect transistor for low‐power applications*. J. Comput. Electron, 19 (Dec. 2019) 271–276. Available: https://doi.org/10.1007/s10825-019-01427-y

[31] A. K. Singh, M. R. Tripathy, S. Chander, K. Baral, P. K. Singh, S. Jit, *Simulation Study and Comparative Analysis of Some TFET Structures with a Novel Partial-Ground-Plane (PGP) Based TFET on SELBOX Structure*. Silicon, 12 (Dec. 2019) 2345–2354. Available: https://doi.org/10.1088/1361-6641/ab542b

[32] S. Kumar, B. Raj, B. Raj, *Dual-Material Gate-Drain Overlapped DG-TFET Device for Low Leakage Current Design*. Silicon, 13 (Jun. 2020)

1599–1607. Available: https://doi.org/10.1007/s12633-020-00547-6

[33] S. Zafar, M. A. Raushan, Sh. Ahmad, M. J. Siddiqui, *Reducing off-state leakage current in dopingless transistor employing dual metal drain*. Semicond. Sci. Technol, 35 (1) (Dec. 2019). Available: https://doi.org/10.1088/1361-6641/ab542b

[34] H. Y. Chang, S. Chopra, B. Adams, J. Li, Sh. Sharma, Y. Kim, S. Moffatt, J. C.S. Woo, *Improved subthreshold characteristics in tunnel field-effect transistors using shallow junction technologies.* Solid State Electron, 80 (Feb. 2013) (59-62). Available: https://doi.org/10.1016/j.sse.2012.10.013

[35] N. Damrongplasit, S. H. Kim, and T. J. K. Liu, *Study of Random Dopant Fluctuation Induced Variability in the Raised-Ge-Source TFET*. IEEE Electron Device Lett, 34 (2) (Feb. 2013) 184-186. Available: https://doi.org/10.1109/LED.2012.2235404

[36] N. Damrongplasit, Ch. Shin, S. H. Kim, R. A. Vega and T. J. K. Liu, *Study of Random Dopant Fluctuation Effects in Germanium-Source Tunnel FETs*. IEEE Trans. Electron Devices, 58 (10) (Oct. 2011) 3541–3548. Available: https://doi.org/10.1109/TED.2011.2161990

[37] B. Ghosh and M. W. Akram, *Junctionless Tunnel Field Effect Transistor*. IEEE Electron Device Lett, 34 (5) (May. 2013) 584–586. Available: https://doi.org/10.1109/LED.2013.2253752

[38] P. K. Asthana, B. Ghosh, Y. Goswami, and B. M. M. Tripathi, *High-Speed and Low-Power Ultra deep-Submicrometer III–V Heterojunctionless Tunnel Field-Effect Transistor*. IEEE Trans. Electron Devices, 61 (2) (Feb. 2014) 479–485. Available: https://doi.org/10.1109/TED.2013.2295238

[39] M. J. Kumar and S. Janardhanan, *Doping-Less Tunnel Field Effect Transistor: Design and Investigation.* IEEE Trans. Electron Devices, 60 (10) (Oct. 2013) 3285–3290. Available: https://doi.org/10.1109/TED.2013.2276888

[40] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy, *Nanowire transistors without junctions*. Nature Nanotechnol, 5 (3) (Mar. 2010) 225–229. Available:

https://doi.org/10.1038/nnano.2010.15

[41] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, *Theory of the Junctionless Nanowire FET*. IEEE Trans. Electron Devices, 58 (9) (Sep. 2011) 2903–2910. Available: https://doi.org/10.1109/TED.2011.2159608

[42] C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, *Junctionless multigate field-effect transistor*. Appl. Phys. Lett. 94 (5) (Jan. 2009) 53511-53513. Available: https://doi.org/10.1063/1.3079411

[43] M. Bolokian, Ali. A. Orouji, A. Abbasi, M. Houshmand. *Pyramid $P^+$ area in SOI junction-less MOSFET for logic applications: DC investigation*. Appl. Nanosci., (Feb. 2023). Available: https://doi.org/10.1007/s13204-023-02808-3

[44] M. Bolokian, Ali. A. Orouji, A. Abbasi, D. Madadi. *Realization of Double-Gate Junctionless Field Effect Transistor Depletion Region for 6 nm Regime with an Efficient Layer*. Phys. Status Solidi., 219 (21) (Nov. 2022) 2200214. Available: https://doi.org/10.1002/pssa.202200214

[45] M. Bavir, A. Abbasi, Ali. A. Orouji. *Performance Enhancement of Asymmetrical Double Gate Junctionless CMOS Inverter With 3-nm Critical Feature Size Using Charge Sheet*. IEEE J. Electron Devices Soc., 10 (Apr. 2022) 334-340. Available: https://doi.org/10.1109/JEDS.2022.3166708

[46] I. Ch. Cherik, A. Abbasi, S. K. Maity, S. Mohammadi. *Junctionless tunnel field-effect transistor with a modified auxiliary gate, a novel candidate for high-frequency applications*. Micro and Nanostructures., 174 (Feb. 2023). Available: https://doi.org/10.1016/j.micrna.2022.207477

[47] *ATLAS Device Simulation Software*, Silvaco, Santa Clara, CA, USA, 2019. Available: https://silvaco.com/

[48] W. Hänsch, T. Vogelsang, R. Kircher, and M. Orlowski, *Carrier transport near the Si/SiO2 interface of a MOSFET*. Solid State Electron. 32 (10) (Oct. 1989) 839-849. Available: https://doi.org/10.1016/0038-1101(89)90060-9

[49] S. Xiong and J. Bokor, *Sensitivity of double-gate and FinFET Devices to*

*process variations*. IEEE Trans. Electron Devices, 50 (11) (Nov. 2003) 2255–2261. Available: https://doi.org/10.1109/TED.2003.818594

[50] J.-P. Colinge, J. C. Alderman, W. Xiong, and C. R. Cleavelin, *Quantum–mechanical effects in trigate SOI MOSFETs*. IEEE Trans. Electron Devices, 53 (5) (May. 2006) 1131–1136. Available: https://doi.org/10.1109/TED.2006.871872

[51] M. Rahimian, *Two Dimensional Analytical Modeling and Simulation for Junctionless Tunneling Field Effect Transistors*, presented at the 7th Int. Conf. Electrical Engineering, Computer Science, & Information Technology, Hamedan, Iran, (2023) Feb. 5-7. Available: https://civilica.com/doc/1638014