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Research Paper

Designing a Novel high-speed ternary-logic multiplier using GNRFET Technology

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Abstract:

This paper presents a novel design of a ternary multiplier based on graphene nanoribbon field-effect transistor (GNRFET). GNRFET, as a new material with superior physical and electronic properties, can be a good choice instead of conventional devices such as metal–oxide–semiconductor field-effect transistor (MOSFET) and CNTFET. Moreover, multiple-valued logic (MVL) can help to reduce area and decrease the computational step compared with binary logic. We proposed a ternary multiplier with the resistors to produce ternary logic. The proposed multiplier performances are analyzed by evaluating the delay, power, and power-delay product (PDP), with 15 nm process technologies based on GNRFET. The simulation results with HSPICE demonstrate that the proposed design framework outperforms state-of-the-art designs in circuit parameters.

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1. INTRODUCTION

Increasing the number of transistors on-chip led to some problems on a semiconductor field-effect transistor (MOSFET). Short channel effect, high power density, and increasing gate leakage are some of these challenges [1-3]. Scientists investigate new materials to solve these problems such as quantum cellular automata (QCA) [4], carbon nanotube field-effect transistor (CNTFET) [5], and graphene nanotube ribbon field-effect transistor (GNRFET). Many research and circuit designs have been done on CNTFET while a few researchers accomplished based on GNRFET.

GNRFET has remarkable properties rather than conventional CMOS. i.e. less short channel effect, larger Ion/I off ratio, larger transconductance [6]. GNRFET introduces as the candidate material for MVL circuit design [7]. Graphene consists of a single layer of atoms arranged in a two-dimensional honey club lattice as an allotrope of carbon. Graphene suffers from a lack of bandgap [8]. There are some ways to open the bandgap in Graphene. One of them is changing [9] to a nanoribbon shape. Graphene nanoribbon has enough bandgap to be used in the transistor. Graphene nanoribbon field-effect transistors with their excellent physical and electronic properties are a suitable replacement for MOSFET and CNTFET.

MVL circuit design is an interesting field for researchers [10-12]. The MVL-based designed circuit has great features including fewer computational steps, interconnections, and less chip area and power consumption. The MVL structures can be used in distinct applications such as decision systems, robotic, and process control [13].

A multiplier is an arithmetic circuit used in distinct computations. The focus of this paper is to implement a high-speed multiplier using GNRFET and compare it with the exiting multiplier, based on circuit parameters including delay, power consumption, and PDP. First of all, we want to investigate some GNRFET based structures. The ternary-based adder structure using GNRFET is proposed in [14]. The length of GNRFET is 15 nm. The simulation results showed that using GNRFET leads to a significantly power-delay product (PDP) reduction ompared with CNTFET. Moreover, the researcher designed a quaternary inverter based on GNRFET which has a good performance [15].

In the reminder of the paper, GNRFET is reviewed in more detail in Section 2. The new proposed design of multiplier based on GNRFET in ternary logic is explained in section 3. Section 4 consists of the extensive simulation results and finally, the paper is concluded in section 5.

2. Graphene Nano Ribbon Field-Effect Transistors

GNRFET is the best material to replace with silicon-based transistors. Graphene and silicon have the same processing methods. The edge of GNR determines GNR type. The graphene nanoribbon is divided into zigzag-edge (ZGNR) and armchair-edge (AGNR) [16]. The structure of AGNR and zigzag carbon nanotube is the same. AGNR has semiconductor behavior and ZGNR depicts metallic behavior. The armchair-edge graphene nanoribbon is a suitable material for designing MVL circuits [17].

The effective parameter for MVL circuit design is the bandgap which is inversely related to the width of GNRFET. The width of a GNR (Wch) is obtained as following [18]

$$W_{ch} = (N+1)\sqrt{3}\frac{dcc}{2} \quad (1)$$

Where N is the dimer lines number. The length of the carbon-carbon bond is dcc= 0.144. Fig. 1 display the structure of the six-ribbon GNRFET.

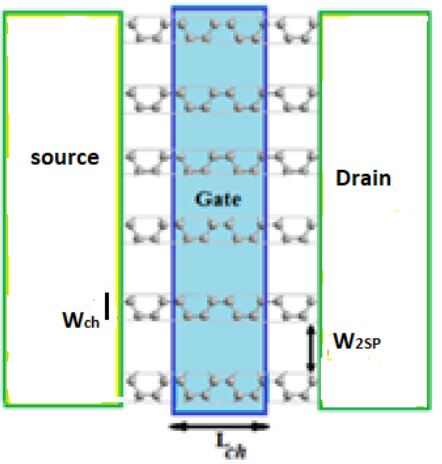


Fig1. Structure of six-ribbon GNRFET [10]

The parameters of the GNRFET [19] their descriptions, and values are shown in Table I.

Table I
The GNRFET parameters

Device parameter	Description	Default value
L	Physical channel length	15nm
Tox	The thickness of the top gate dielectric material (planer gate)	0.95nm
2Wsp	The spacing between the edges of two adjacent GNRs within the same device	2 nm
NRib	The number of GNRs in the device	6
P	The edge roughness percentage of the device	0
Dop	Source and drain reservoirs doping fraction	0.001
Tox2	Oxide thickness between channel and substrate/bottom gate	20nm
Gates_tied	Whether gate or sub hold the same voltage	0

3. The proposed design

There is a total of 2^2=4 functions in binary logic whereas there is 3^3=27 functions in ternary logic. More computation can be implemented in smaller area using Ternary logic rather than binary logic. Ternary logic has 3 voltage levels including 0, 1/2 VDD, VDD, as it can be seen in Table II [20]. The truth table of the ternary multiplier are shown in Table III. If A=2, B=2, Carry is 1 else carry is =0. If A or B= 0, the product is 0 and if A and B are 1 or 2, the result is 1. If A=1 and B=2 or A=2 and B=1, the product is 2.

Table II

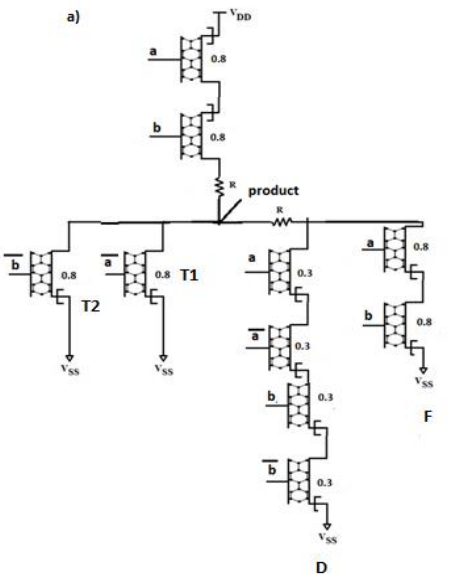
LOGIC SYMBOLS

Logic value	Voltage value
0	0
1	1/2 V_{DD}
2	V_{DD}

Table III
The truth table of ternary multiplier

A	B	Product	Carry
0	0	0	0
0	1	0	0
0	2	0	0
1	0	0	0
1	1	1	0
1	2	2	0
2	0	0	0
2	1	2	0
2	2	1	1

The proposed ternary multiplier circuit based on GNRFETs is shown in Fig.2. As it can be seen in this figure, part *a* represents the required structure for production, and part *b* is the Carry output. There are two resistors that VDD voltage is divided into 3 parts,0,0.45,0.9V. If A=0 or B=0, T1 or T2 are on and the product becomes 0. On the other hand, If A=B=1 or A=B=2, Part D or F of Fig 2 become on and the result of the product is one. The amount of the Carry is 1 when A and B are 2, otherwise, the carry is 0.



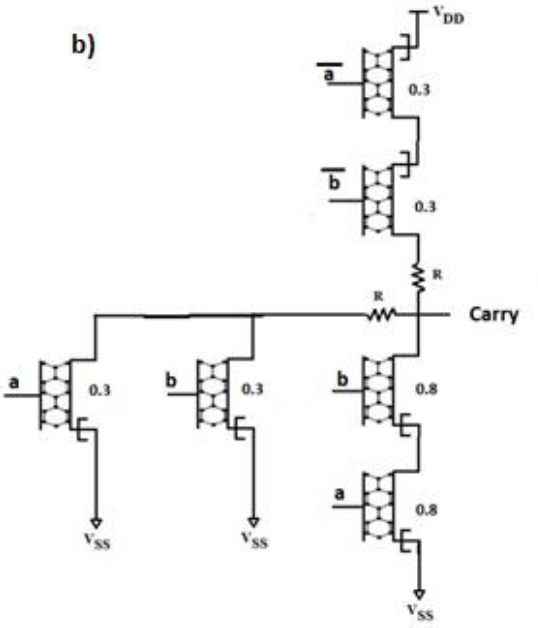


Fig 2. The proposed ternary multiplier circuit using GNRFETs: a) product, b) carry.

The transient response of the proposed multiplier design is illustrated in Fig3. Results indicate that our design has a better performance in PDP.

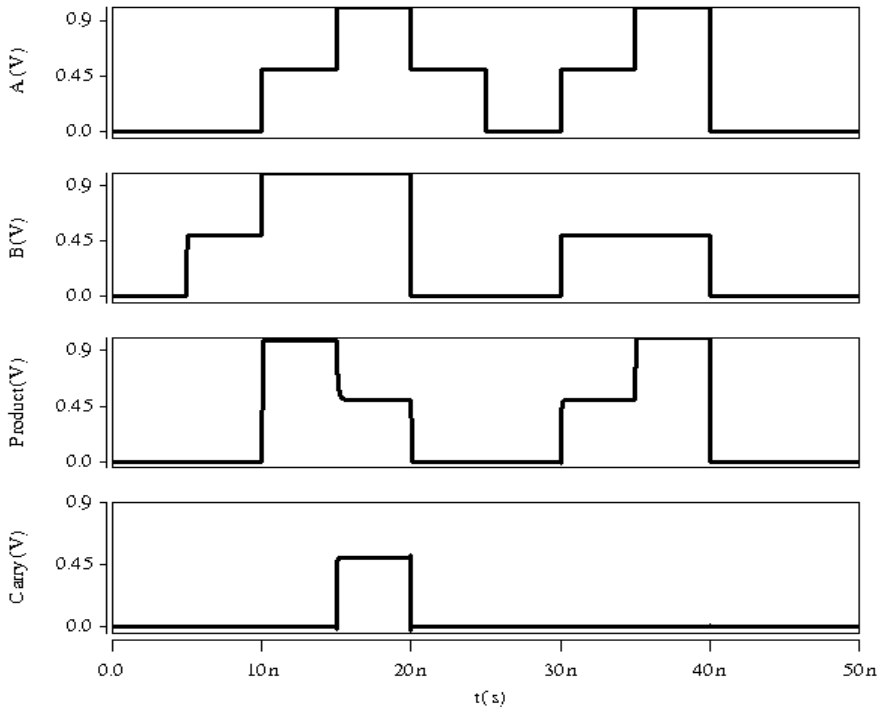


Fig 3. Transient response of multiplier design

High-speed multipliers are critical for many digital filtering applications. one of the most important circuits in digital systems with high-performance is high-speed multiplication.

To achieve the highest possible speed, array multipliers, rather than conventional sequential add-and-shift multipliers, must be used. Our emphasis in this paper is on the speed to increase it as much as it is possible without facing unpredictable problems. The performances of the proposed multiplier are analyzed by evaluating the delay, power, and power-delay product (PDP) parameters, using 15 nm GNRFET technologies. Extensive simulations are performed using the HSPICE synopsis. Results are shown in Table IV. The suggested design has the best delay and PDP compared with CNTFET-based multipliers.

Table IV.
THE SIMULATION RESULT OF THEPROPOSED DESIGN AND COMPARISON

	Power (uw)	Delay (e-12s)	PDP (e-16j)
Proposed design	4.32	15.36	0.66
Ref [20]	0.66	169	1.16
Ref [21]	4.16	42.3	1.75
Ref [22]	0.9598	95.195	0.913

For the analysis of the proposed design, PDP and temperature are investigated. As it can be seen in Fig4 PDP and Power do not change while increasing the temperature.

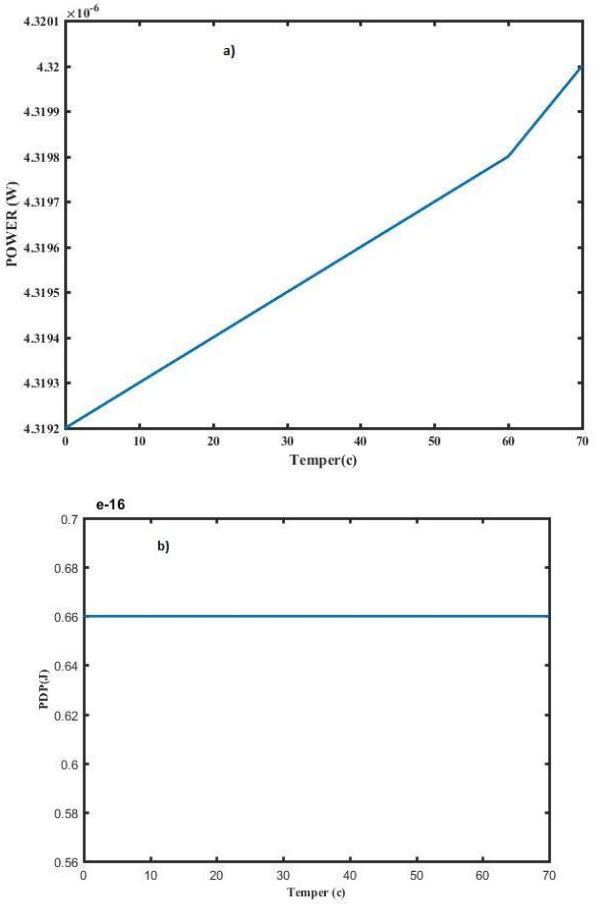


Fig4: a) Power as a function of temperature, b) PDP as a function of temperature.

4. CONCLUSION

GNRFET with excellent physical and electrical characteristics can be a good choice for circuit design. GNR has a high conducting capacity. The bandgap of GNR is inversely related to its width. Two types of GNR are Armchair and Zigzag. Due to the semiconductor behavior of Armchair GNR, utilized in circuit design. In this paper, the multiplier is designed based on GNRFET and its performance is investigated based on different parameters for the first time. Transient responses confirm that our proposed design has a correct performance. Our proposed design was compared with the CNTFET multiplier design. The extensive simulation results represent that the multiplier based on the proposed design framework outperforms state-of-the-art designs in-circuit measurements. GNRFET can be a suitable material for MVL circuit design.

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