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Improvement of the Drive Current in 5nm Bulk-FinFET Using Process and Device Simulations

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Abstract: We present the optimization of the manufacturing process of the 5nm bulk-FinFET technology by using the 3D process and device simulations. In this paper, by simulating the manufacturing processes, we focus on optimizing the manufacturing process to improve the drive current of the 5nm FinFET. The improvement of drive current is one of the most important issues in the FinFETs design. We first investigate the impact of manufacturing process parameters include gate oxide thickness, type of the gate oxide, height of fin, and doping of the source and drain region on threshold voltage, breakdown voltage, and drive current of the transistor. Then, by selecting the optimal parameters of the manufacturing process, we improve the drive current of the 5nm bulk-FinFET.

Keywords: FinFET, Manufacturing Process, Drive Current, Threshold Voltage, DIBL Effect.

1. INTRODUCTION

The scaling down of transistors give advantages such as improving circuit performance, increasing speed, and lower running costs per function. One of the big challenges for CMOS semiconductor components is the issue of scaling and power consumption. In standard flat MOSFET, a channel is located between the source and the drain that covers the gate electrode by an insulator (SiO_2) [1]. This action causes the electrostatic control of the channel by the gate through the capacitance between the gate and the channel area [2]. By reducing the length of the channel, which is accompanied by a decrease in the depths of the source and the drain regions, the effects of the short channel appear. These

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effects reduce the threshold voltage, the transconductance, the saturation and linear drain current, the carrier mobility in the channel [3], the subthreshold slope, and the drain induced barrier lowering (DIBL) [4, 5] and increase the off-state current of the transistor. The technological solution to reduce the effects of short channels in integrated circuits is the use of the FinFETs instead of classic transistors [6].

The FinFET is made on a silicon-based substrate. The FinFET body consists of two gates and a channel that is perpendicular to the wafer's surface. Therefore, the electrostatic control of the gateway on the channel has been improved. In this transistor the direction of the current is parallel to wafer surface. In very small devices like FinFETs, quantum effects appear due to the narrow dimensions of the transistor. Therefore, the behavior of these transistors cannot be explained by classical mechanistic approaches. Instead, we have to go to the quantum mechanics approaches [7]. Among these effects, there is the effect of quantum confinement and volume inversion. The quantum effects affect the mobility of the carriers and the threshold voltage of the FinFETs [8]. Hence, the carrier mobility for the FinFET is more than for conventional MOSFET structures [9]. For low values of the electric field, the electron drift velocity in the channel increases with increasing the electric field. These drift velocities are saturated in high electric fields, which is called velocity saturation effects [10]. In such high electric fields, velocity saturation occurs that affects the I-V characteristics of the MOSFET [11, 12]. It has been observed that for the same gate voltage, with lower values of the source-drain voltage, the MOSFET becomes saturated and the saturation current decreases [13]. Due to higher vertical electric fields, channel carriers are dispersed in the oxide interfaces. This will reduce the mobility of the carriers and reduce the current [14].

In FinFET structure, the substrate doping can be kept low and the short channel effects can be controlled. Due to the lower doping of substrate, the mobility is less affected by scattering. Therefore, the FinFET structures offer various advantages such as a higher mobility, lower threshold voltage, better subthreshold slope, lower short channel effect (SCE) and DIBL than a conventional MOSFET structure.

It has already been found experimentally that the drive current of SOI-FinFETs is efficiently improved by mobility enhancement with the stress liner technique [15] and by reduction of parasitic resistance using a raised source and drain (RSD) with selective epitaxial growth technique [16].

Also, the high drive current with low leakage current bulk-FinFET has been realized using optimization of the channel profile [17]. Recently, the FinFETs with High-κ Spacers have been reported for improvement of drive current [18].

In this paper, we focus on optimizing the process of manufacturing a 5 nm FinFET structure through channel change, changing the source and drain doping rate, changing the thickness of the oxide layer and the type of oxide to improve the drive current by maintaining other specifications. This is the ability to calculate the dependence of the fundamental parameters of the transistor on the manufacturing variables.

2. THE FINFET STRUCTURE

A FinFET is a variation in double gate MOSFET where an ultra-thin silicon substrate is made vertical and controlled by self-aligned gates. In FinFET structure, the entire gate electrodes are defined and created on both sides of the substrate at the same time. Hence, the problem of alignment faced in double gate structure is solved in the FinFET structure. The schematic structure of the bulk-FinFET is shown in Fig. 1.

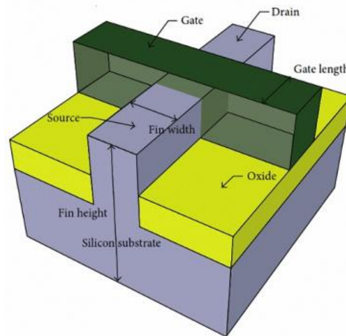

Fig. 1. The schematic structure of the bulk-FinFET.

Another benefit of FinFETs is that their channel is not doped. This is a very important feature in terms of reducing the size of the transistor (reducing the length of the channel). Because in doped channels, the number of impurities in the channel should be reduced proportionately with decreasing channel length, thus causes in the destruction of the threshold voltage and the degradation of transistor performance**.** While in FinFETs due to lack of impurities, the reduction in channel length does not result in these problems [19]. On the other hand, in these devices, the fin can be very narrow, that means that there is no area in the channel that is out of control. Also, the power dissipation in this transistor is low because when the transistor is off there is no leakage path for carriers and source-drain current**.** The drain current for a MOSFET transistor is given by:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V\right)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (1)$$

Here W is the in the channel width. For a FinFET transistor, channel width can be given as follows:

$$W = 2 \times Fin\,Height + Fin\,Width \quad (2)$$

Therefore, the fin height is a factor in increasing the drive current of the transistor, and with its increase, the drain current of the transistor can be increased [20].

One of the effects of a short channel is called DIBL, which refers to lowering the threshold voltage at higher drain voltage levels. If the gate voltage is not sufficient for the inversion, that is $V_G<V_T$, the carriers will encounter a potential barrier in the channel, that can block the current. By increasing the gate voltage, this potential barrier disappears. But for short channel devices, such a potential barrier is controlled by both V_{GS} and V_{DS} voltages [21]. If the drain voltage increases, the depletion layer increases in size and extends below the gate. Therefore, the potential barrier decreases in the channel, which leads to the transport the electrons between the source and the drain, and a lower threshold voltage is required. This reduction in threshold voltage with channel length is called the $V_{TRoll\text{-}off}$. The current that occurs under these conditions is called the subthreshold current (off-state current). The DIBL increases the drain current by increasing the drain voltage even in the saturated [22]. There is a simple tool called voltage-doping transform (VDT), which can be used to interpret the effects of small device parameters such as gate length or drain voltage to electrical parameters. In the specific cases of SCE and DIBL, the following expressions can be extracted from the VDT model [23].

$$SCE = 0.64\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left[1 + \frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{bi} \quad (3)$$

$$DIBL = 0.8\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left[1 + \frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{DS} \quad (4)$$

where L_{el} is the electrical (effective) channel length, V_{bi} is the source or drain built-in potential, t_{ox} is the gate oxide thickness, x_j is the source and drain junction depth and t_{dep} is the penetration depth of the gate field in the channel

region, which is equal to the depth of the depletion region underneath the gate in a bulk MOSFET. Based on the above expressions, the $V_{TRoll\text{-}off}$ of a MOSFET with a given channel length L_{el} can be calculated using the following relationship:

$$V_{TRoll-off} = V_{TH\infty} - SCE - DIBL \quad (5)$$

where $V_{TH\infty}$ is the threshold voltage of a long channel device. As can be seen from these expressions, short-channel effects can be minimized by reducing the junction depth and the gate oxide thickness. They can also be minimized by reducing the depletion depth through an increase in doping concentration. However, in modern devices, the practical limitations of junction depth and thickness of gate oxide have caused a significant increase in the effects of the short channel and excessive amounts of DIBL [24]. If the channel length is small compared to the depletion layer, the effects of the short channel are intolerable and limit the ability to achieve further reduction along the gate. To control this effect, according to the reduction in channel length can be reduced. By channel doping concentration or increasing the gate capacitance or both, these effects can be controlled. The capacitance of the gate determines the gate control on the channel. Eq. (6) shows that the gate capacity can be increased by scaling (reducing) the thickness of the oxide of the gate. It has been observed that a device with a thinner oxide gate has less depletion layer, hence the SCE profile is improved [25].

$$C_{ox} \propto \frac{\varepsilon_{ox}}{t_{ox}} \quad (6)$$

The thickness of the oxide layer should be scaled to the channel length. But if the thickness of the oxide is reduced further, the carrier tunneling phenomenon will dominate, which will increase the leakage current of the gate to an unacceptable level [26]. Therefore, the only remaining option is the choice of dielectric materials with a high dielectric constant to increase the oxide capacitance. Since the thicker dielectric layers can be used, the capacitance of the high gate-oxide is achieved. This thicker layer also causes less carrier tunneling. The SiO_2 has a dielectric constant of 3.9, but hafnium is a material that has dielectric constant of 25, which is 6 times higher than SiO_2 [27]. Therefore, by changing the type of dielectric to the hafnium, this can be achieved.

3. SIMULATION AND RESULTS

We have simulated a 5 nm bulk-FinFET manufacturing process by using 3D Silvaco TCAD simulators. In order to simulate, first, the masks of different stages of the manufacturing processes were designed using the mask editor (MaskViews). Then, the stages of manufacturing process were defined in the VictoryProcess environment. Finally, the VictoryDevice simulator was used to obtain the electrical parameter of the designed FinFET.

Fig. 2(a) shows a created silicon substrate with impurity of boron at a rate of 5×10^{14} cm^{-3} and direction of crystalline (100) by using a SUB mask. To create the fin of the transistor, the silicon was etched from the sides of the substrate with 85 degrees and filled these areas with silicon oxide using ACIVE mask. Then, with the same mask, a silicon layer was created with a 10 nm thickness in the middle of the structure and was doped with concentration of 1×10^{14} cm^{-3} by ion implantation process. Also, the diffusion process was performed to correct damaged atoms and penetrate more impurities. The result is shown in Fig. 2(b).

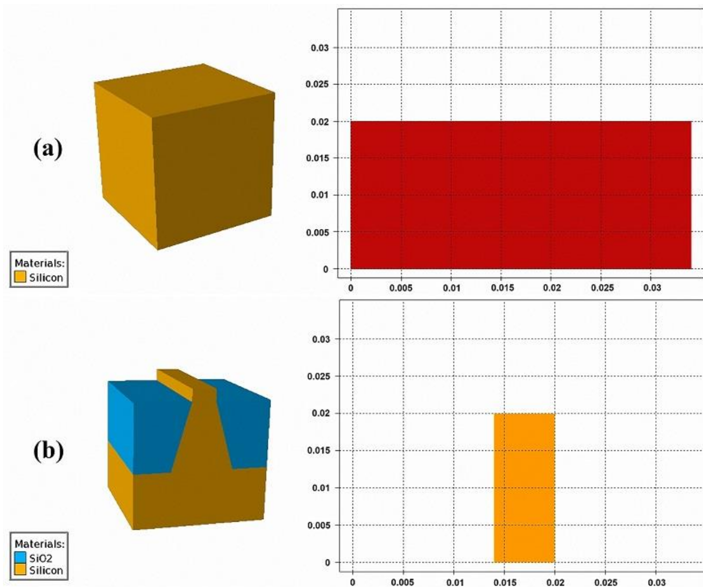

Fig. 2. (a) Create a silicone substrate using the USB mask
(b) Forming the fin for the device using the ACTIVE mask.

At this point in the process, a nitride insulator layer with a thickness of 0.5 nm placed on the structure. Next, a layer of polysilicon with thickness 5 nm was placed on the nitride layer. At the end of this part, the two sides of the

polysilicon were removed using a POLY mask, as shown in Fig. 3(a). In this step, it is necessary to separate the gate polysilicon from the source and drain regions. For this purpose, a layer of oxide thickness of 2.7 nm was placed on the entire structure. Next, the oxide placed on the polysilicon gate was removed using the SD_ETCH mask. Furthermore, the excess oxide on both sides of the structure and the nitride addition in the same area were removed. The structure after these processes is shown in Fig. 3(b).

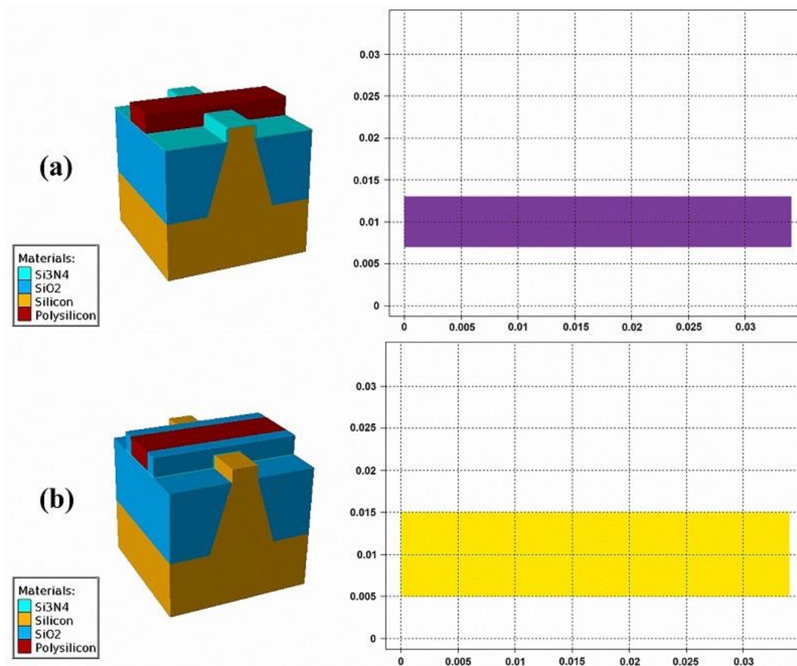

Fig. 3. (a) Create a gate area using the POLY mask.
(b) Create spacer using the SD_ETCH mask.

In the next step, the goal is to create the source and drain region. First, a photoresist layer with 20 nm thickness was deposited in the target area using the CONT mask. Then a layer of polysilicon with a thickness of 14 nm was placed on the source and drain areas, and next the photoresist layer was removed. Now the created source and drain areas should be doped. Two stages of ion implantation process with angles of 0 and 180 degrees with the impurity rate of 2×10^{16} cm^{-3} and the energy of 10 KeV on the source and drain areas were performed. Following the ion implantation process, the annealing process was performed at a temperature of 1050℃ and for 5 seconds. Finally, the gate, drain

and source electrodes created by using the CONT mask. The resulting structure is shown in Fig. 4.

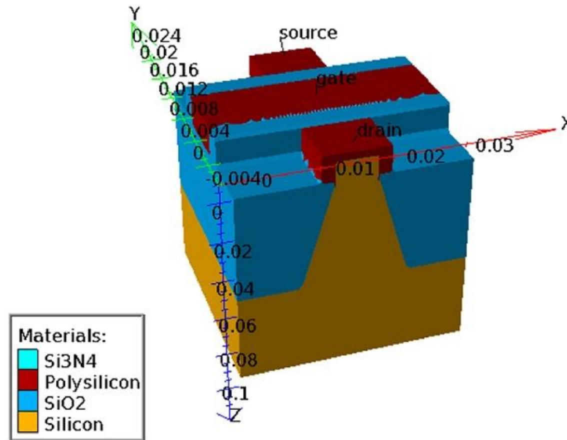

Fig. 4. Cross section of the device after final process step.

After completing the manufacturing process simulation for the 5nm bulk-FinFET using the VictoryProcess tools, we now obtain several structural parameters of the device by VictoryDevice simulator. Fig. 5(a) shows the drain current versus gate voltage plot. The threshold voltage (V_T) is extracted from this curve by the following relation:

$$V_T = (maximum\,slope\,to\,the\,curve\,of\,drain\,current\,vs.\,gate\,voltage) - (Half\,drain\,voltage\,applied) \quad (7)$$

The results obtained from this graph shows that the threshold voltage of the device is about 0.275 V.

In order to calculate the transconductance (g_m) of the transistor, it was necessary to calculate the diagram slope of the drain current versus the gate voltage. From the drain current vs. the gate voltage graph, transconductance vs. gate voltage was extracted as shown in Fig. 5(b). The results show that maximum transconductance of the transistor is 9 μ℧ corresponding to gate voltage of 0.5 V.

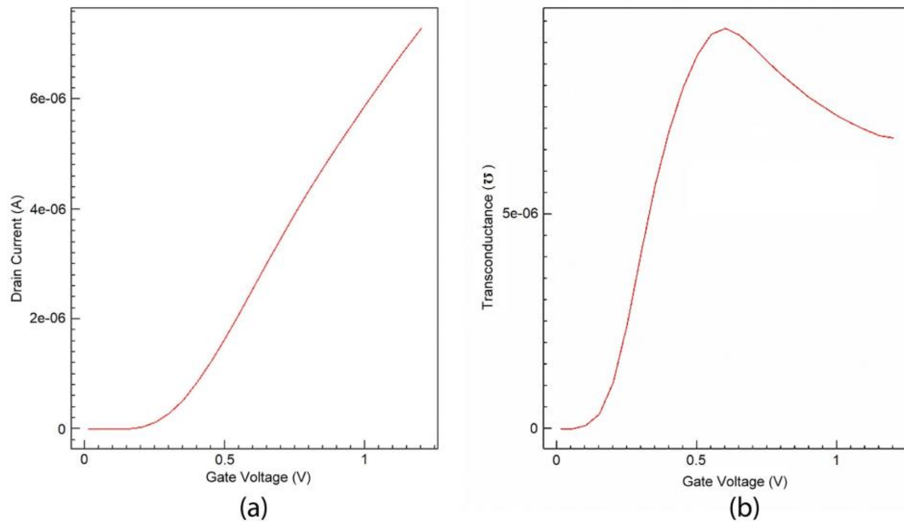

Fig. 5. (a) Drain current versus gate voltage. (b) Transconductance versus gate voltage.

Also, to calculate the cutoff frequency, we plot the current gain vs. frequency. The point where the current gain is zero is known as the cutoff frequency. As shown in Fig. 6(a), the cutoff frequency of the transistor is about 200 MHz. In order to calculate the breakdown voltage, we should change gate voltage to zero. Fig. 6(b) shows the drain current versus drain voltage for $V_g= 0$.

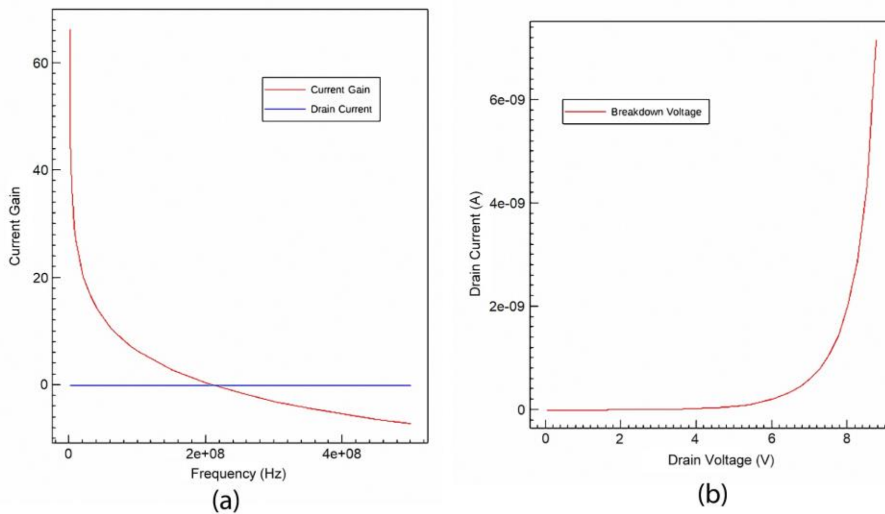

Fig. 6. (a) Current gain as a function of frequency. (b) Drain current versus drain voltage for Vg=0.

The voltage at which the current is reached to 1×10^{-9} A is known as the breakdown voltage of the transistor. The results obtained from this graph shows that breakdown voltage of the device is about 7.43 V.

Increasing the drain voltage leads to the reduction of a potential barrier of the channel and hence effectively reduces the threshold voltage, this is known as DIBL effect. In the FinFET structures, the gate has better control over the channel region and hence DIBL is much reduced compared to the conventional MOSFET structures. A coefficient defined as η describes the effect of DIBL. η can be calculated from the measurement of V_T at the different drain to source voltages as follows:

$$\eta = \frac{dV_T}{dV_{DS}} \tag{8}$$

This coefficient is calculated from two values of V_T.

1- In V_{DS} low, (V_{DS}=0.05 V or 0.1 V), which is called V_{Tlin} (The linear part of the characteristic I-V).

2- In normal V_{DS} or high ($V_{DS}=V_{DD}$) called V_{Tsat} (the saturation part of curve I-V).

$$\eta = \frac{V_{Tsat} - V_{Tlin}}{V_{DD} - 0.1} \tag{9}$$

Fig. 7(a) shows the drain current as a function of gate voltage for two V_{DS} values of 1.2 V and 0.1 V, which gives us two threshold voltages. By substituting these values in equation (9), η of the device was obtained of about 8.1 mV.

In order to obtain the drive current of the FinFET, the drain current versus drain-source voltage diagram was plotted for V_{GS}=0.6 V. As shown in Fig. 7(b), the drive current of the transistor in V_{DS}=0.5 V is equal to 4.7 µA.

4. REFINING PROCESSES TO IMPROVE THE DRIVE CURRENT

In this section, we improve the drive current by refining the process effective factors, whereas other parameters such as threshold voltage, breakdown voltage, cut-off frequency, transconductance and DIBL have not been deviate from the desired value. As the FinFET drive current depends on several manufacturing process factors, by changing the oxide thickness, changing type of oxide, changing doping of the source and drain regions, and changing the fin height, the drive current has been increased.

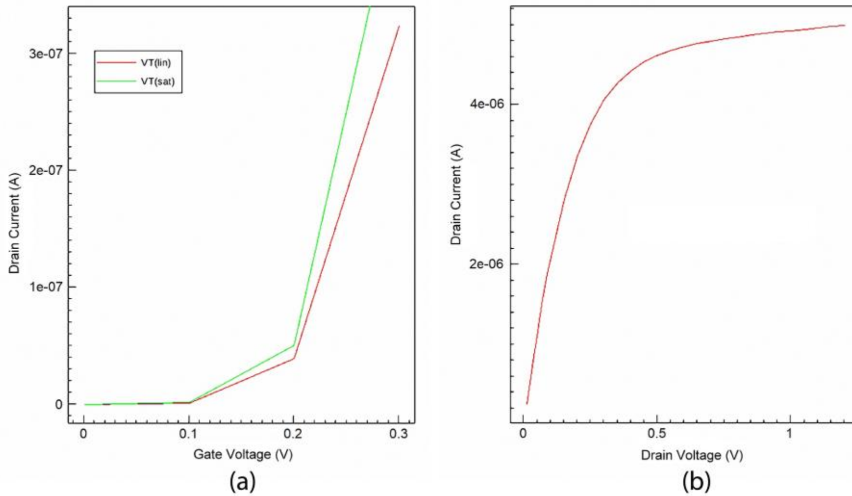

Fig. 7. (a) Drain current vs. gate voltage for two values of the drain-source voltage. (b) Drain current vs. drain voltage plot for V_{GS}=0.6 V.

First, the thickness of the gate oxide was reduced from 0.5 nm to 0.45 nm. The further reduction of oxide thickness, the leakage current of the gate has been increased. Then, the type of oxide to the hafnium (HfO2) was changed, which has the highest dielectric constant among the available materials. In the next step, the fin height from 10 nm to 12 nm was increased. To further increase the fin height, we get out of the 5 nm technology. Finally, the amount of impurities was increased in the source and drain regions from 2×10^{16} cm^{-3} to 4×10^{16} cm^{-3}. Since the breakdown voltage and the resistive on-mode of the transistor are dependent on the concentration of impurities in the source and drain regions, the choice of impurities concentration was done based on their quantities. The results obtained with these changes are shown in Fig. 8 to Fig. 12.

Fig. 8 shows the effect of changing the parameters of the manufacturing process on the threshold voltage. As can be seen, by changing the thickness of the gate oxide, the threshold voltage was converted to 0.284 V. By changing the type of oxide, the threshold voltage was converted to 0.262 V. By changing the fin height, the threshold voltage was converted to 0.293 V, and by increasing the amount of impurities, the threshold voltage was converted to 0.237 V. Therefore, changing parameters within the mentioned range did not have much effect on the threshold voltage of the transistor.

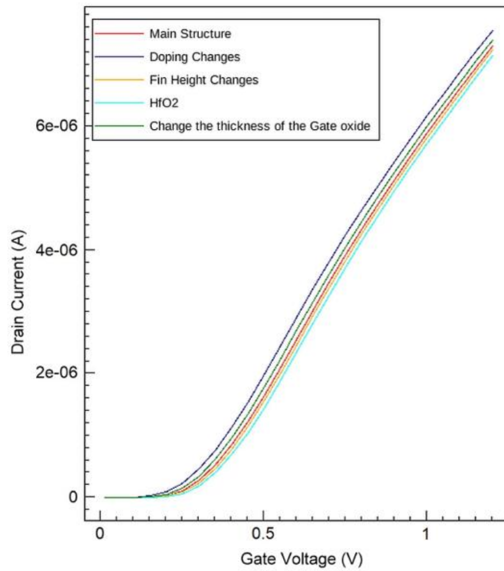

Fig. 8. Effect of change of manufacturing parameters on the threshold voltage.

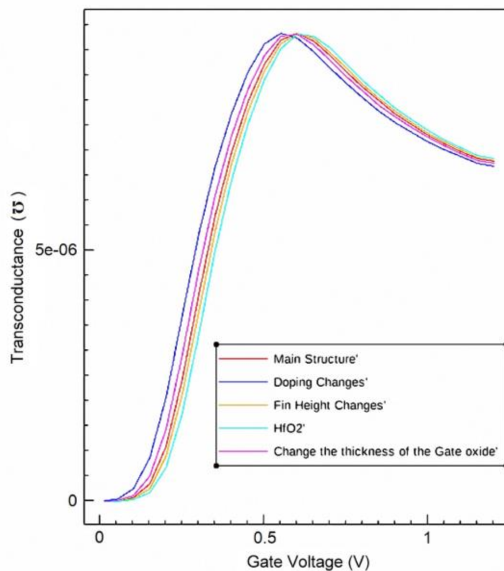

Fig. 9. Effect of change of manufacturing parameters on the transconductance.

The effect of changing the parameters of the manufacturing process on the transconductance of the FinFET is shown in Fig. 9. As shown in this Figure, the

change of all the items mentioned in the manufacturing process the g_m parameter did not changed significantly, and equal to the same amount of 9 μʊ.

Fig. 10 shows the effect of changing the parameters of the manufacturing process on the cutoff frequency of the transistor. As one can see, no appreciable change in the cutoff frequency is observed and is equal to 200 MHz.

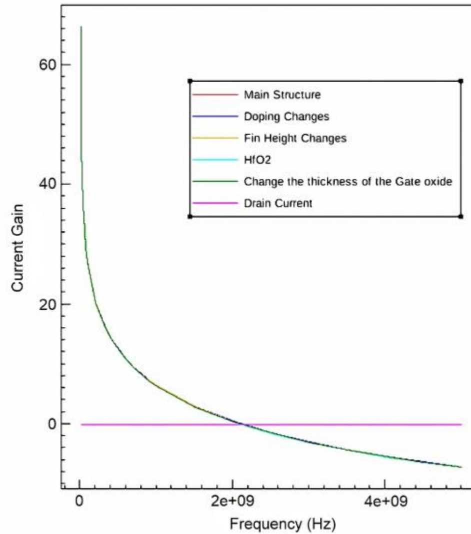

Fig. 3. Effect of change of manufacturing parameters on the cutoff frequency.

Fig. 11 shows the breakdown voltage of the transistor after applying changes in manufacturing process parameters. As can be observed, by decreasing the thickness of the gate oxide, the breakdown voltage slightly decreases and was converted to 7.3 V. By changing the type of oxide, the breakdown voltage slightly increases and was converted to 7.56 V. By changing the height of the fin, the breakdown voltage was converted to 7.5 V, and changing the amount of impurity, the breakdown voltage was converted to 7.23 V, which is not a significant change. Also, we calculated the DIBL parameter after applying changes in manufacturing process parameters. By changing the thickness of the gate oxide layer, DIBL changes to 9.2 mV. By changing the type of oxide, DIBL changes to 7.8 mV. By changing the height of the fin, DIBL changes to 8.7 mV and changing the amount of impurity DIBL changes to 7.5 mV. Hence, there are no significant changes and DIBL parameters remain nearly constant.

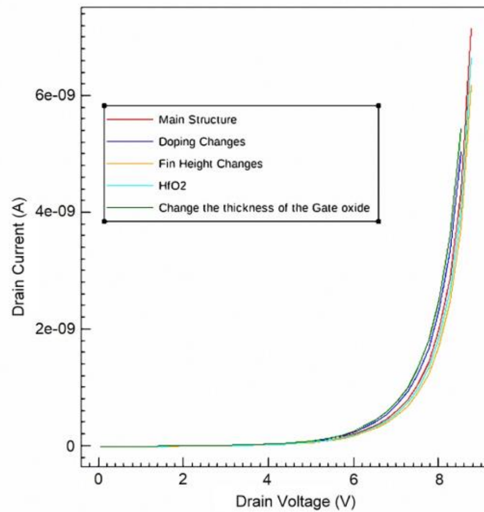

Fig. 4. Effect of change of manufacturing parameters on the breakdown voltage.

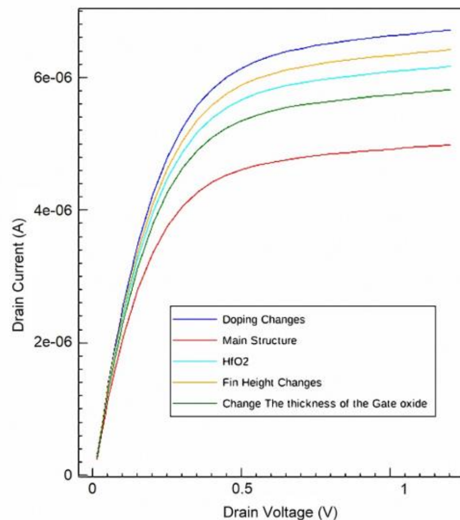

Fig. 5. Effect of change of manufacturing parameters on the drive current.

However, Fig. 12 shows that changing the manufacturing process parameters has a great impact on the drive current of the FinFET. As shown in this figure, by reducing gate oxide thickness, the drive current of the FinFET at V_{GS}=0.6 V increases and reached to 5.45 µA. Also, by changing the gate oxide to the HfO_2, the drive current increases to 5.78 µA. Furthermore, drive current of the

transistor reached 6 μA by increasing the height of the fin. Finally, by increasing the doping of source and drain regions, the drive current will reach to 6.3 μA. Therefore, by optimization of manufacturing processes, we were able to increase drive current of the FinFET compared to the initial structure. In this work, by optimizing all of manufacturing process parameters, the drive current of the FinFET at V_{GS}=0.6 V increased to 6.3 μA.

5. CONCLUSION

In this paper, we have presented improvement of the drive current in 5nm bulk-FinFET using optimization of the manufacturing process. The simulation results show that by selecting the optimal parameters of the manufacturing process such as gate oxide thickness, type of the gate oxide, the height of fin and the doping rate of the source and drain regions, we have increased the drive current of the 5nm FinFET to 6.3 μA at V_{GS}=0.6 V. In addition, we tried to keep the other parameters of the FinFET such as the threshold voltage, the breakdown voltage, and the cut-off frequency within their normal range in this optimization. The designed 5nm bulk-FinFET structure could be a feasible option for future CMOS technology.

REFERENCES

[1] K. Pourchitsaz and M. R. Shayesteh, *Self-heating effect modeling of a carbon nanotube-based fieldeffect transistor (CNTFET)*, *Journal of Optoelectronical Nanostructures* 4 (1) (2019, Jan.) 51-66.

[2] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, T. Elewa, *Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance*, IEEE Electron Device Letters 8 (9) (1987, Sep.) 410-412.

[3] O. Semenov, A.Vassighi, M. Sachdev, A. Keshavarzi, CF. Hawkins, *Effect of CMOS technology scaling on thermal management during burn-in*, IEEE transactions on semiconductor manufacturing 16 (4) (2003, Nov.) 686-695.

[4] G. Saini, AK. Rana, *Physical scaling limits of FinFET structure: A simulation study*, International Journal of VLSI design & communication Systems (VLSICS) 2 (1) (2011, Mar.) 26-35.

[5] M. Roohy, and R. Hosseini, *Performance Study and Analysis of Heterojunction Gate All Around Nanowire Tunneling Field Effect Transistor*, *Journal of Optoelectronical Nanostructures* 4 (2) (2019, May.) 13-28.

[6] SP. Mohanty, *Nanoelectronic mixed-signal system design*, New York: McGraw-Hill Education, 2015, 78-94.

[7] W. Han, *Toward Quantum FinFET*, ZM. Wang, editor. Springer, 2013, 54-67.

[8] P. Mishra, A. Muttreja, N. K. Jha, *FinFET circuit design, in Nanoelectronic Circuit Design*, Springer, 2011, 23–54.

[9] R. Das, R. Goswami, and S. Baishya, *Tri-gate heterojunction SOI Ge-FinFETs*, Superlattices Microstruct 91 (2016, Mar.) 51–61.

[10] V. E. Dorgan, M.-H. Bae, and E. Pop, *Mobility and saturation velocity in graphene on* SiO_2, Applied Physics Letters 97 (8) (2010, Aug.), 82112.

[11] A. T. M. Fairus, V. K. Arora, *Quantum engineering of nanoelectronic devices: the role of quantum confinement on mobility degradation*, Microelectronics Journal, 32 (8) (2001, Aug.) 679–686.

[12] B. Azizollah-Ganji, and M. Gholipour, *Effects of the channel length on the nanoscale field effect diode performance*, Journal of Optoelectronical Nanostructures 3 (2) (2018, Jun.) 29-40.

[13] V. K. Arora, *Theory of scattering-limited and ballistic mobility and saturation velocity in low-dimensional nanostructures*, Current Nanoscience 5 (2), (2009, May.) 227–231.

[14] V. Kilchytska, S. Makovejev, S. Barraud, T. Poiroux, J.-P. Raskin, D. Flandre, *Trigate nanowire MOSFETs analog figures of merit*, Solid-State Electronics, 112, (2015, Oct.) 78–84.

[15] N. Collaert, A. De Keersgieter, K. G Anil, and et al., *Performance improvement of tall triple gate devices with strained SiN layers*, IEEE electron device letters 26 (11) (2005, Oct.) 820-822.

[16] J. Kedzierski, *High-performance symmetric-gate and CMOS compatible Vt asymmetric-gate FinFET devices*, in IEDM Tech. Dig., (2001) 437-440.

[17] T. Kanemura, T. Izumida, N. Aoki, M. Kondo, and et al., *Improvement of drive current in bulk-FinFET using full 3D process/device simulations*, In IEEE International Conference on Simulation of Semiconductor Processes and Devices (2006, Sep.) 131-134.

[18] A. Sachid, C. Min-Cheng, and H. Chenming , *FinFET With High-κ Spacers for Improved Drive Current*. IEEE electron device letters 37(7) (2016, May.) 835-838.

[19] X. Wang, A. R. Brown, B. Cheng, and A. Asenov, *Statistical variability and reliability in nanoscale FinFETs*, in Electron Devices Meeting (IEDM), 2011 IEEE International, (2011, Dec.) 4–5.

[20] I. Ferain, C. A. Colinge, and J.-P. Colinge, *Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors*, Nature 479 (7373), (2011, Nov.) 310.

[21] C. H. Wang, P.-F. Zhang, *Three-dimensional DIBL for shallow-trench isolated MOSFET's*, IEEE Transactions on Electron Devices 46 (1) (1999, Jan.) 139–144.

[22] *Threshold voltage roll-off compensation using back-gated MOSFET devices for system high-performance and low standby power*, by H. I. Hanafi, R. H. Dennard, W. E. Haensch. (2006, Aug.) Google Patents [Online]. Available:https://patents.google.com/patent/US7089515B2/en

[23] T. Skotnicki, *Heading for decananometer CMOS-Is navigation among icebergs still a viable strategy?*, in Solid-State Device Research IEEE (2000, Sep.) 19–33.

[24] S. Sengupta, S. Pandit, *Study of LER/LWR induced V T variability of an EδDC n-channel MOS transistor*, in Devices for Integrated Circuit (DevIC) (2017, Mar.) 685–689.

[25] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C. H. Choi, *A 45nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging*, in Electron Devices Meeting (2007, Dec.) 247–250.

[26] C. H. Jan, U. Bhattacharya, R. Brain, S.J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, *A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications*, in Electron Devices Meeting (IEDM) (2012, Dec.) 1–3.

[27] M. Radosavljevic, G. Dewey, J. M. Fastenau, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, *Non-planar, multi-gate InGaAs quantum well field effect transistors with high-k gate dielectric and ultra-scaled gate-to-drain/gate-to-source separation for low power logic applications*, inElectron Devices Meeting (IEDM) (2010, Dec.) 1–6.