Self-heating effect modeling of a carbon nanotube-based field-effect transistor (CNTFET)

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Abstract: We present the design and simulation of a single-walled carbon nanotube (SWCNT)-based field-effect transistor (FET) using Silvaco TCAD. In this paper, the self-heating effect modeling of the CNT MOSFET structure is performed and compared with conventional MOSFET structure having same channel length. The numerical results are presented to show the self-heating effect on the *I–V* characteristics of the CNT MOSFET and conventional MOSFET structures. Results from numerical simulation show that the maximum temperature rise and the performance degradation of the CNT MOSFET are quite lower than that of the conventional MOSFET counterpart. These advantages are contributed by the good electrical and thermal properties of the SWCNTs. Therefore, SWCNT materials have a high capability for the development of active devices with low power dissipation and good reliability at high operating temperature.

1. INTRODUCTION

In recent years, despite the rapid growth of electronics manufacturing technology and entry into the nanotechnology frontier, there are many challenges in the design of electronic circuits. Some of these challenges relate to the process of manufacturing electronic integrated circuits and the need to reduce the size of transistors. On the other hand, the scaling down of the silicon-based FET leads to some problems and critical challenges such as short channel effect, increasing the gate leakage current, and high power density [1, 2]. In order to overcome these limitations, carbon nanotube field effect transistor

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(CNTFET) has introduced a promising device due to the unique structure and excellent electrical properties [3-5].

Since the discovery of the nanotubes by Samio Iijima from NEC Corporation in 1991 [6], many researchers were studied on the structure and applications of these materials due to their electrical, thermal and mechanical properties [7, 8]. Todays, nanotechnology has achieved significant progress in fabrication of various devices at nanometer regime such as molecular diodes and the carbon CNFETs. This has provided new opportunities for VLSI circuits to achieve continuing cost minimization and performance improvement in a post silicon-based-CMOS technology area. The CNT-based FET devices are getting more and more importance today due to improved I-V characteristics and high channel mobility are considered as a replacement for future semiconductor devices [9- 11].

The self-heating is a major problem in the MOSFETs that affects on the performance and specification of the devices. The self-heating can affect on the *I–V* characteristics, threshold voltage, turn-on time, signal delay, and cutoff frequency of the transistors. In the conventional MOSFET structures, the low thermal conductivity of the silicon and SiO_2 layer inhibits cooling in the device and causes severe strong self-heating effects. This results in higher channel operating temperatures and is evidenced by the negative differential conductance at high gate biases that is characteristic of these devices. The device mobility is reduced as a result of the elevated temperatures and results in reduced maximum drain saturation current. Moreover, the temperature rise leads to more serious reliability problems such as increased electromigraton and enhanced impact ionization and causes the performance degradation of the devices.

The single-walled CNTs were suggested that could have a thermal conductivity much larger than that of the silicon material, which are connected to their phonon thermal transport properties. Therefore, the self-heating effects in the CNT-based MOSFET can be reduced due to excellent electrothermal properties of the CNTs.

Recently, the self-heating effects in semiconducting CNT-based devices have been studied in some works. Generally there are two methods for developing thermal models of the MOSTETs. The first method consists of the calculations of the thermal gradient inside the device and drain-source current. Physical models of the temperature dependence of transistor parameters must take into account a number of physical factors such as the energy gap, the state density at the conduction and valence band edge, the dielectric constant, the electron saturation velocity, the carrier mobility, and the Schottky barrier height. Therefore, model expressions become very complicated and it results rather

heavy from a computational point of view. The second method is based on a semi-empirical approach, where some of the fitting parameters of the large signal model are dependent on the temperature according to empirical relationships including fitting parameters having a physical meaning. However, the semi-empirical model requires the electrical characterisation of devices and the befitting procedure of parameters extraction.

In this paper, we investigate the self-heating effect in a CNT- based MOSFET and compare to a conventional MOSFET structure using Silvaco TCAD software. The ATLAS simulator implements Wachutka's thermodynamically rigorous model of lattice heating, which accounts for Joule heating, heating and cooling due to carrier generation and recombination, and the Peltier and Thomson effects in the devices. Also, the ATLAS simulator accounts for the dependence of material and transport parameters on the lattice temperature.

The rest of this paper is organized as follows. Section 2 describes the CNT-based FET structures. In section 3, we present the employed theoretical model for simulation of the CNT MOSFET. Section 4 covers the simulation results obtained for the characteristics of the CNT MOSFET. Finally, we conclude this paper in section 5.

2. STRUCTURE OF CNT-BASED FET

The CNT-based FET can be structurally divided into the top gate and bottom gate. Two possible structures of CNT-based FET are shown in figure 1(a) and (b). In the structure with bottom gate, the device has two metal electrodes as the source and drain and a CNT layer is on the wafer and plays channel's role. In the top gate structure, the gate is located above the CNT layer. The top gate structures have better advantages than bottom gate structures.
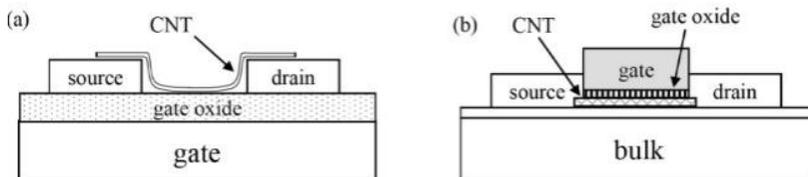
Fig. 1. (a) Bottom-gate structure   (b) Top-gate structure

On the other hand, as shown in Fig. 2, the CNT-based FET can have structures, depending on the type of connection. These two types of structures

are the CNT Schottky barrier MOSFET [12] and CNT MOSFET [13]. In the CNT-based Schottky barrier MOSFET, the gate voltage controls the width of the Schottcky in the source. Thus, the tunneling in the source channel controls the current of the transistor. In this structure, there is a bipolar conductivity. But in the CNT-based MOSFET, the gate voltage controls the channel conductivity. The impurity of the source and drain in this type of transistor prevents the transmission of electrons and holes, therefore, leads to its monopolar conductivity.

   The most important problem of the CNT-based SBMOSFET is the existence of Schottcky barrier between the CNT and the junction of the source and the drain, which leads to a large subthreshold slope and bipolar conduction in the nanoscale devices. This limits the on-current of the device and increases the off-current in an exponential range, both of which are unacceptable for high performance and low power consumption. In contrast, the CNT-based MOSFETs have a high efficiency and low off-current. Therefore, in the work, we design and simulation of an SWCNT-based MOSFET.
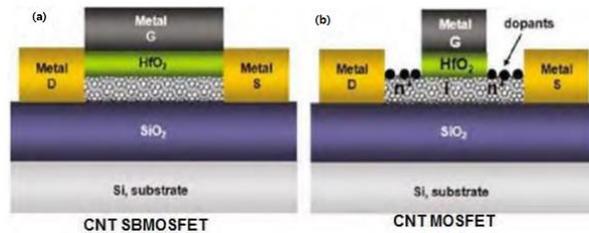
Fig. 2. CNT-based transistor   (a) Schottky barrier MOSFET   (b) MOSFET

A. *Carbon Nanotube Structure*

   The CNTs are composed of hollow cylinders in which carbon molecules are arranged in a honeycomb lattice, which have unique properties and are used for applications such as nanoelectronics and optical electronics. The characteristics of the nanotubes depend on their structure and can act as metal or semiconductor according to the chiral vector. The most pertinent quantities defining CNTs are the characteristics of the CNT's chiral vector C_h. The chiral vector C_h is a vector in the unrolled CNT's honeycomb lattice defined as:

$$c_h = na_1 + ma_2 \equiv (n,m) \tag{1}$$

where n and m are integers and a_1 and a_2 are the lattice defining vectors of graphene. The values of n and m determine the length L of C_h, which is the circumference of the CNT, and the chiral angle θ. The chiral angle is the angle between the chiral vector (n, m) and the zigzag direction of the honeycomb lattice $(n, 0)$. These two properties are integral in defining a CNT's electrical characteristics. Certain combinations of L and θ give semiconductor characteristics, while others induce metallic characteristics. The unit cell of a CNT is the rectangular region bounded by the chiral vector C_h and the vector T. The vector T is the one-dimensional translation vector of the CNT that extends from the origin of the C_h vector to the first lattice point B in the honeycomb lattice. In more simplified terms, the point B is the first carbon atom in the honeycomb lattice that is intersected by the line propagating in the normal direction to C_h. The vector T is defined similarly to C_h as

$$T = t_1 a_1 + t_2 a_2 \equiv (t_1, t_2) \tag{2}$$

where t_1 and t_2 are integers. Based on the properties of their C_h and T vectors, CNTs can be divided into one of three structural categories known as the armchair, zigzag, and chiral. A CNT falls into these three categories based on its chiral angle θ, which can vary from zero to thirty degrees. At the boundaries of θ, zigzag CNTs have a chiral angle of zero degrees, while armchair CNTs have a chiral angle of thirty degrees. Chiral CNTs have a chiral angle that lies anywhere between but not including zero and thirty degrees. These basic structural properties are the properties that govern each individual CNT's physical properties [14]. These properties determine how a CNT will act in electrical applications.

Another feature of the CNTs, which affects their electrical properties, is the number of walls. According to Fig. 3, the CNTs come in three forms when actually grown, single-walled carbon nanotubes (SWCNTs), double-walled nanotubes (DWCNTs) and multi-walled carbon nanotubes (MWCNTs). SWCNTs are structured with one layer of graphene rolled into a CNT. But MWCNTs are contrastingly composed of multiple layers of graphene rolled in the same manner. The main difference between the single-wall and multi-wall nanotubes is the diameter of the nanotubes. The SWCNTs are a huge potential for applications in electronics due to their metallic and semiconductor properties and the ability to carry high current [15]. The diameter of the CNT can be approximated as

$$d_{CNT} = \frac{\sqrt{3a_0}}{\pi} \sqrt{n^2 + m^2 + nm} \tag{3}$$

where a_0 is the distance between two atoms. Also, in the case of semiconducting CNT, the bandgap energy is given by:

$$E_G \propto \frac{0.8ev}{d_{CNT}(nm)} \tag{4}$$
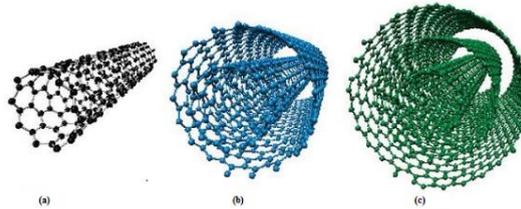
Fig. 3. Different types of CNTs   a) Single-wall b) Two-wall   c) Multi-wall

The SWCNT allows electrons to travel more distances without dispersion. The average distance in which metal CNT can carry electrons is estimated to be about 100 nm, which is much higher than copper connections, which allow only 40 nm to pass electrons along the path. Most notably, SWCNTs were found to have maximum current densities two to three times greater than metals commonly used as conductors. Also, SWCNTs have excellent mechanical properties, in addition to their elegant electronic properties. Their strong mechanical strength makes them a good choice for making flexible electronic components. Today, SWCNTs have attracted much interest in the scientific society due to their excellent electrical, thermal, and mechanical properties. Different groups of CNT-based FETs have reported on flexible substrates with an efficiency ranging from 40 MHz to 6 GHz.

3. PHYSICAL MODELS

Although the electron transport in a CNT-based FET is quasi-ballistic, the effect of phonon scattering cannot be ignored, which plays an important role in its performance [16]. The joule heating along the channel region is mainly caused by phonon scattering during its operation. The temperature variation has a strong effect on its scattering strength, which further affects the electron transport in the CNT-based FET and hence self-heating gives a feedback on the

electron transport [17]. Therefore, one of the important problems that effect on performance and characteristics of the devices is self-heating effects.

The phonon transmission occurs in the presence of a defect in the semiconductor forbidden gap. This is essentially a two-stage process. The recombination rate is given by the well-known Shockley-Read- Hall expression [18, 19]:

$$R_{SRH} = \frac{pn - n^2_{ie}}{\tau_{p_0}[n + n_{ie} \, exp\left(\dfrac{E_{TRAP}}{kT_L}\right)] + \tau_{n0}[p + n_{ie} \, exp\left(\dfrac{-E_{TRAP}}{kT_L}\right)]} \qquad (5)$$

where τ_{po} and τ_{no} are the minority carrier lifetimes (proportional to the density of defect levels) and E_{TRAP} is the difference between the energy level of the defect and the intrinsic form of the surface, k is the Boltzmann constant, and the T_L (K) is the lattice temperature. Therefore, self-heating effects depend on electron transport and non-uniform distribution of temperature. On the other hand, for a semiconducting SWCNT, the current contributed by the carriers at different energy states are different [20, 21].

In the semiconductor devices, the lattice heat flow equation is the following:

$$C\frac{\partial T_L}{\partial t} = \nabla(\kappa \nabla T_L) + H \qquad (6)$$

where C is the heat capacitance per unit volume. κ and H are the thermal conductivity and the heat generation, respectively. The key material dependent parameters in Equation 6 are the thermal conductivity and the heat capacity. In general, both thermal conductivity and heat capacity are both composition and temperature dependent.

In this paper, a CNT MOSFET structure has been simulated using self-heating simulator of the Silvaco TCAD and compared with the conventional MOSFET structure. The self-heating simulator extends ATLAS tools to account for lattice heat flow and general thermal environments. This simulator accounts for the dependence of material and transport parameters on the lattice temperature. The self-heating simulator implements Wachutka's thermodynamically rigorous model of lattice heating, which accounts for Joule heating, heating and cooling due to carrier generation and recombination, and the Peltier and Thomson effects.

4. SIMULATION AND RESULTS

The schematic structure of CNT MOSFET with a single channel is shown in Fig. 4(a). Under the metal gate, there is a gate dielectric material SiO_2, and the SWCNT is grown on the bulk silicon oxide SiO_2. The SWCNT channel is undoped, and the other regions are heavily doped, serving as the source and drain parts of the CNTFET, respectively. The metal gate controls the intrinsic channel region through the gate dielectric SiO_2, and the source and drain metals serve as two electrodes. Fig. 4 (b) shows the conventional MOSFET structure which effective channel length of both the structures has been kept the same. The CNT MOSFET and conventional MOSFET device parameters as defined by our structure are given in Table I.
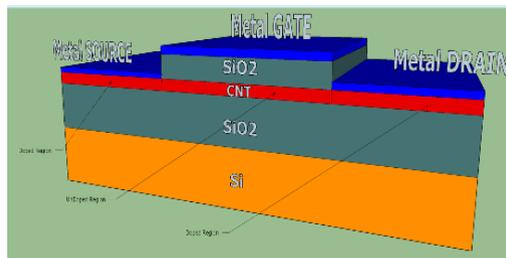
(a)
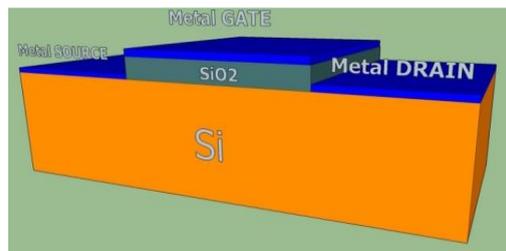
(b)

Fig. 4. (a) SWCNT MOSFET Structure   (b) Conventional MOSFET structure

TABLE I
Structural parameters for CNT MOSFET and conventional MOSFET

Parameters	CNT MOSFET	Conventional MOSFET
gate oxide thickness	5 nm	5 nm
gate length	500 nm	500 nm
Source/Drain Doping	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Gate work function	4.65 eV	4.65 eV
CNT thickness	2 nm	-
Substrate Doping	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}

Devices simulation starts by designing CNT MOSFET and conventional MOSFET structures using ATLAS. There are several steps in devices simulation in order to obtain the characteristics of the transistors for further analysis. The transfer characteristics (I_D versus V_{GS} curve) and output characteristics (I_D versus V_{DS} curve) for both transistor structures will be obtained. Also, there will be some extraction parameter such as threshold voltage (V_T) and maximum drain current (I_{Dsat}). Furthermore, in this paper, special attention is focused on the self-heating effect in the CNT MOSFET structure and compared with the conventional MOSFET. Therefore, the *I–V* characteristics of both transistor structures are characterized and compared for both self-heating and no self-heating cases.

In order to obtain accurate calculation results, the various physical models with fitting material parameters have been used to perform an analysis in ATLAS. For numerical simulations, Newton and GUMMEL (maximum trap 4) models have been used. This section represents and analyzes the simulation results obtained using SILVACO TCAD.

Fig. 5 (a) and (b) shows the drain current versus gate voltage plot of the CNT MOSFET and conventional MOSFET, respectively. The threshold voltage (V_T) which has been extracted from these curves is about 0.74 V and 0.43 V for the CNT MOSFET and conventional MOSFET, respectively. Also, simulation results show that the subthreshold slope for CNT MOSFET is larger than for a conventional MOSFET. This results in faster switching for the CNT MOSFET devices.

The turn-on delay time was obtained to be 300 μs and 360 μs for the CNT MOSFET and conventional MOSFET, respectively. In addition to, from the simulated the CNT MOSFET and conventional MOSFET structures, the cut-off frequency was extracted to be 18 GHz and 16 GHz for the CNT MOSFET and conventional MOSFET, respectively.

(a)

(b)
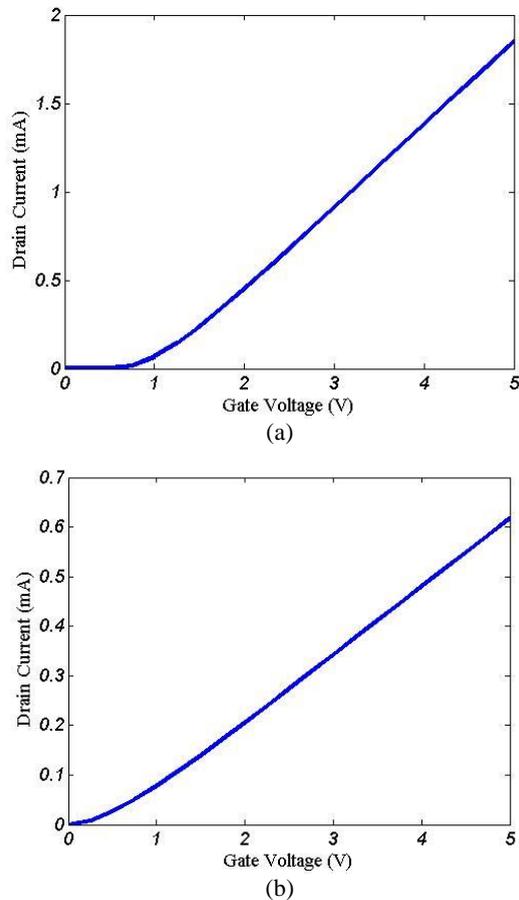
Fig. 5. Drain current vs. gate voltage plot for   (a) CNT MOSFET   (b) Conventional MOSFET

In this work, we have also investigated the effects of self-heating on the devices. Figure 6 shows the internal temperature of the device versus drain voltage plot of the CNT MOSFET and the conventional MOSFET. As can be observed, in both structures, the internal temperature of the device increases with an increase in the drain voltage due to self-heating effect. However, the self-heating effect for CNT MOSFET is less than for a conventional MOSFET.

In CNT MOSFET, self-heating effect can be decreased due to the high thermal conductivity of the CNT layer. Distribution of temperature inside the CNT MOSFET and conventional MOSFET is shown in Fig. 7 (a) and (b) respectively. As indicated in this figure, the high thermal conductivity of the CNT layer leads to a better heat release from the device and hence reducing the self-heating effect on the transistor performance.
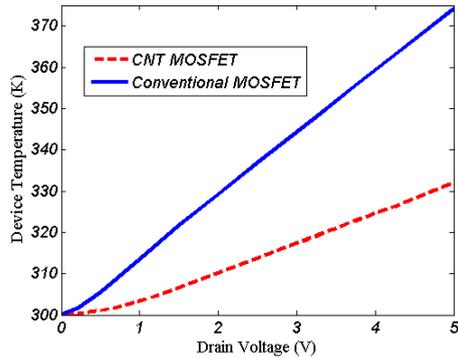
Fig. 6. The internal temperature of the device vs. drain voltage for CNT MOSFET and Conventional MOSFET
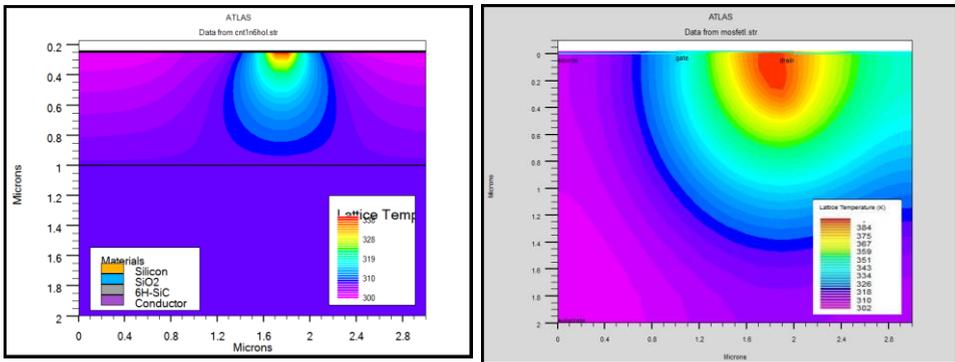
(a)   (b)

Fig. 7. Distribution of temperature inside the device (a) CNT MOSFET   (b) Conventional MOSFET

Fig. 8 (a) and (b) indicate *I-V* characteristics with and without the self-heating effect for the CNT MOSFET and conventional MOSFET, respectively. As can be seen in this figure, the self-heating effect on the *I–V* characteristics of the CNT MOSFET is much smaller in comparison with the conventional MOSFET counterpart. Such a conclusion is consistent with that described in [22] for different CNTFET structures. The comparison between different CNT MOSFET and conventional MOSFET parameters is given by Table II.
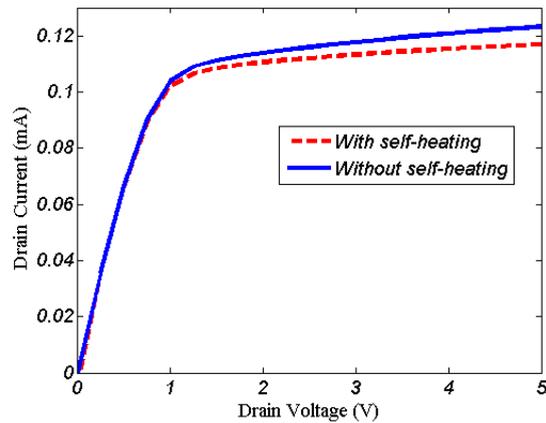
(a)
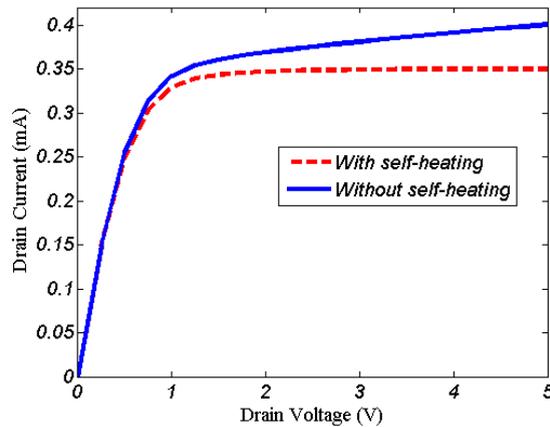
(b)

Fig. 8. I-V characteristics with and without the self-heating effect   (a) CNT MOSFET (b) Conventional MOSFET

TABLE II
Comparison between the CNT MOSFET and conventional MOSFET

Parameters	CNT MOSFET	Conventional MOSFET
Threshold Voltage (V)	0.74	0.43
I_{Dsat} (V_{GS}=3 V)	900 µA	400 µA
Maximum temperature rise (V_{DS}=5 V)	33 K	80 K
Cutoff frequency	18 GHz	16 GHz
Turn-on time	300 µs	360 µs

5. CONCLUSION

In this paper, the self-heating effect in a CNT MOSFET has been investigated and compared to a conventional MOSFET structure having the same effective channel length. The *I–V* characteristics of the CNT MOSFET are characterized and compared for both self-heating and no self-heating cases. It has been demonstrated that the maximum temperature rise, as well as the performance degradation of the CNT MOSFET, is much lower than of the conventional MOSFET counterpart. These advantages are contributed by good electrical and thermal properties of the SWCNTs. Therefore, they have a high capability in the development of advanced active devices with low power dissipation, high operating temperature, and high power applications.

REFERENCES

[1] M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakami, T. M. Tsuno, T. Mihara, K. Shibahara, and S. Miyazaki, *Limit of Gate Oxide Thickness Scaling in MOSFETs due to Apparent Threshold Voltage Fluctuation Induced by Tunnel Leakage Current*. IEEE Transactions on Electronic Devices 48 (2) (2009, Feb) 259- 264.

[2] A. Rezaei, B. Azizollah-Ganji, and M. Gholipour, *Effects of the channel length on the nanoscale field effect diode performance*. Journal of Optoelectronical Nanostructures 3 (2) (2018, Jun) 29-40.
Available: http://jopn.miau.ac.ir/article_2862.html

[3] J. Appenzeller, *Carbon nanotubes for high-performance electronics: Progress and prospect*. Proceedings of the IEEE 96 (2) (2008, Feb) 201–211.

[4] A. Svizhenko, M. P. Anantram, and T. R. Govindan, *Ballistic transport and electrostatics in metallic carbon nanotube.* IEEE Transactions on Nanotechnology 4 (5) (2005, Sep) 557–562.

[5] S. K. Sahoo, G. Akhilesh, R. Sahoo, and M. Muglikar, *High-Performance Ternary Adder Using CNTFET*. IEEE Transactions on Nanotechnology 16 (3) (2017, May) 368-374.

[6] S. Iijima, *Helical microtubules of graphitic carbon*. nature 354 (6348) (1991, Nov) 56.

[7] E. Pop, *Energy dissipation and transport in nanoscale devices*. Nano Resaerch 3 (3) (2010, Mar) 147–169.

[8] M. Akbari Eshkalak, and R. Faez. *A Computational Study on the Performance of Graphene Nanoribbon Field Effect Transistor*. Journal of Optoelectronical Nanostructures 2 (3) (2017, Aug) 1-12.

Available: http://jopn.miau.ac.ir/article_2427.html

[9] G. F. Close, S. Yasuda, B. Paul, S. Fujita, and H. S. P. Wong, *A 1 GHz integrated circuit with carbon nanotube interconnects and silicon transistors*. Nano Letters 8 (2) (2008, Feb) 706–709.

[10] S. J. Wind, J. Appenzeller, R. Martel, V.P.P.A. Derycke, and P. Avouris, *Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes*. Applied Physics Letters 80 (20) (2002, May) 3817-3819.

[11] M. Nayeri, P. Keshavarzian, M. Nayeri, *A Novel Design of Penternary Inverter Gate Based on Carbon Nano Tube*. Journal of Optoelectronical Nanostructures 3 (1) (2018, Jan) 15-26.

Available: http://jopn.miau.ac.ir/article_2820.html

[12] J. Guo, S. Datta, and M. Lundstrom, *A numerical study of scaling issues for Schottky-barrier carbon nanotube transistors*. IEEE transactions on electron devices 51(2) (2004, Feb) 172-177.

[13] M. Hayati, A. Rezaei, and M. Seifi, *CNT-MOSFET modeling based on artificial neural network: Application to simulation of nanoscale circuits*. Solid-State Electronics 54 (1) (2010, Jan) 52-57.

[14] Y. J. Liu and X. L. Chen, *Evaluations of the effective material properties of carbon nanotube-based composites using a nanoscale representative volume element*. Mechanics of materials 35 (1-2) (2003, Jan) 69-81.

[15] W. C. Chen, W. Y. Yin, L. Jia, and Q. H. Liu, *Electrothermal characterization of single-walled carbon nanotube (SWCNT) interconnect arrays*. IEEE Transactions on Nanotechnology 8(6) (2009, Nov) 718–728.

[16] J. Guo and M. Lundstrom, *Role of phonon scattering in carbon nanotube field-effect transistors*. Applied Physics Letters 86 (19) (2005, May) 193103.

[17] Y. Ouyang and J. Guo, *Heat dissipation in carbon nanotube transistors*. Applied Physics Letters 89 (18) (2006, Oct) 183122.

[18] W. Shockley, and W. T. Read Jr, *Statistics of the recombinations of holes and electrons*. Physical review 87 (5) (1952, Sep) 835.

[19] R. N. Hall, *Electron-hole recombination in germanium*. Physical review 87 (2) (1952, Jul) 387.

[20] J. W. Mintmire and C. T. White, *Universal density of states for carbon nanotubes*. Physical Review Letters 81 (12) (1998, Sep) 2506.

[21] C. J. Xing, W. Y. Yin, L. T Liu, and J. Huang, *Investigation on self-heating effect in carbon nanotube field-effect transistors*. IEEE Transactions on Electron Devices 58 (2) (2011, Feb) 523-529.

[22] S. Hasan, M. A. Alam, and M. S. Lundstrom, *Simulation of carbon nanotube FETs including hot-phonon and self-heating effects*. IEEE Transactions on Electron Devices 54 (9) (2007, Sep) 2352–2361.