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Switching Performance of Nanotube Core-Shell Heterojunction Electrically Doped Junctionless Tunnel Field Effect Transistor

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Abstract: In this paper, a novel tunnel field effect transistor (TFET) is introduced, that due to its superior gate controllability, can be considered as a promising candidate for the conventional TFET. The proposed electrically doped heterojunction TFET (EDHJTFET) has a 3D core-shell nanotube structure with external and internal gates surrounding the channel that employs electrostatically doping rather than ion-implantation for creating the tunneling junction. The staggered type InAs/$GaAs_{0.1}Sb_{0.9}$ heterojunction devices, considerably amplifies the band to band tunneling rate. The effect of device geometry and physical design parameters on the performance of the device are comprehensively investigated and cut off frequency of 200GHz, on/off current ratio of 9.41×10^{8} and subthreshold swing of 8.7 mV/dec are achieved. The sensitivity analysis reveals that core/shell control gate workfunction and doping density are critical design parameters that may affect the device performance. Moreover, the insensitivity of off-state current to the drain voltage variation and channel length scaling signifies the application of this device in nanoscale regime.

Keywords: Junctionless transistor, Tunnel field effect transistor, Band to band tunneling, Subthreshold swing, Gate workfunction.

1. INTRODUCTION

Nowadays, the development in semiconductor technology is aiming towards reducing the dimensions of metal-oxide-semiconductor field effect transistor (MOSFET) for achieving high performance low power integrated circuits. However, as the channel length scales down to be comparable to the distance between source/channel and drain/channel depletion regions, short channel effects occur which ultimately degrade the device switching performance [1-4]. The main current mechanism of conventional MOSFET is based on drift-diffusion transport, in which carriers pass over the gate modulated potential

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barrier at the source/channel interface. However, the minimum room temperature subthreshold swing of MOSFET is limited at 60mV/dec. Tunnel field effect transistor (TFET) is introduced as a potential candidate for the traditional speed by delivering subthreshold swing lower than 60mv/dec with improved switching speed. By definition, TFET is a gated reverse biased p-i-n diode in which carriers tunnel through the source/channel junction via band to band tunneling (BTBT) approach [5-6]. However, besides all the merits, low on-state current of TFET has been discussed as a concerning problem. Recently, particular attention is dedicated for heterojunction TFET using III-V as well as IV strained junctions like Ge-Si and SiGe-Si, which provides relatively smaller tunneling barrier [7-8]. Generally, in heterojunction structure with staggered type band alignment, a wide bandgap semiconductor is merged together with a narrow band gap material, which ultimately provides improved on-state current. In addition, the smaller carrier effective mass, the higher probability of tunneling current is expected. However, the conventional TFET requires complex fabrication process due to the formation of physically doped P-i-N regions. Basically, random dopant fluctuations at the source/channel interface leads to the degradation of subthreshold swing and degradation of on-state current [9-13]. In recent researches, a particular focus is dedicated to electrical doping rather than physical doping in which the charge type and its relative density are exactly modulated by the appropriate employment of external polarity controlled electric field [14-15]. Basically, increasing the gate control over the tunneling junction can provide superior improvement in the on-state current as well as reducing short channel effects. Clearly, nanotube core-shell structure with external shell gate as well as internal core gate surrounding the channel is an electrostatically optimized device that can effectively increase the drain drive current [16-22].

In this paper, the positive aspects of nanotube core-shell structure and planar electrically doped TFET are combined to design a novel 3D nanotube core-shell electrically doped heterojunction junctionless TFET (EDHJTFET), which can be beneficial for p-channel applications seeking low power steep-slope characteristics with enhanced on-state drive current. The main feature of the proposed junctionless structure is the similar doping profile from source to drain which facilitates fabrication process of the device. The proposed heterojunction structure has InAs material in the source region and $GaAs_{0.1}Sb_{0.9}$ in the channel and drain regions, respectively. Basically, mixed arsenide–antimonide based heterojunctions are gaining much attention as they provide a lattice-matched interface as well as a wide range of compositionally controllable tunneling barrier. The electrical characteristics of the device is comprehensively investigated and impact of different physical and geometrical parameters that

may influence the scaling and main electrical measures of the device are assessed via statistical analysis. In the first step, one design parameter is varied, while other parameters are considered constant and following that, standard deviation and mean value of each electrical measures are calculated for that specific parameter. The sensitivity value which is calculated as the standard deviation over mean value in percentile reflects significant variation of device performance with respect to a particular design parameter. The paper is organized as follows: the device structure and simulation models are introduced in section 2. Following that, in section 3, the electrical performance of EDHJTFET is thoroughly investigated via conducting a comprehensive sensitivity analysis. Finally, the paper is summarized in section 4.

2. SIMULATION SET UP AND DEVICE SCHEMATIC

The 3D schematic of the proposed EDHJTFET is presented in Fig.1(a) and the 2D cross section of the device in the on-state operation clarifying the band to band tunneling direction is illustrated in Fig. 1(b). The device has P^+-P^+-P^+ doping profile along the device from source to channel. However, the main merit of the device is the employment of opposite gate biases for electrically doping of the regions without the need for ion-implantation. The proposed structure has two gates surrounding the channel and source region, respectively. The control gate (V_{CG}) is located over the channel region, which is responsible for modulating the channel charge density. In addition, the polarity gate (V_{PG}) with similar metal gate workfunction is placed over the source region with opposite bias with respect to the control gate, inducing opposite charge. The primary design parameters are as follows: the control core/shell gate workfunction as well as the polarity gate workfunction are 4.7eV. The primary hole density along the device for source, channel and drain region is $8\times10^{18}cm^{-3}$. In addition, 2nm of HfO_2 is considered for the gate insulator. The channel radius (r) is 5nm, the channel length (L_{ch}) is 25nm and the source and drain length is 20nm. The numerical simulations are carried out via ATLAS device simulator [23] and following models are activated for comprehensive performance assessment of the device: (a) In principle, for p-type operation of the device band to band tunneling occurs from the source conduction band minima to the channel valence band maxima; thus nonlocal band to band tunneling model is taken into account. (b) By definition, direct band to band tunneling phenomena, characterizes the carrier generation in the high field tunneling region without any impression of local defects and traps. However, in the presence of related traps energy states, the excessive tunneling leakage current besides degradation of subthreshold swing is established before the incident of control gate assisted band to band tunneling.

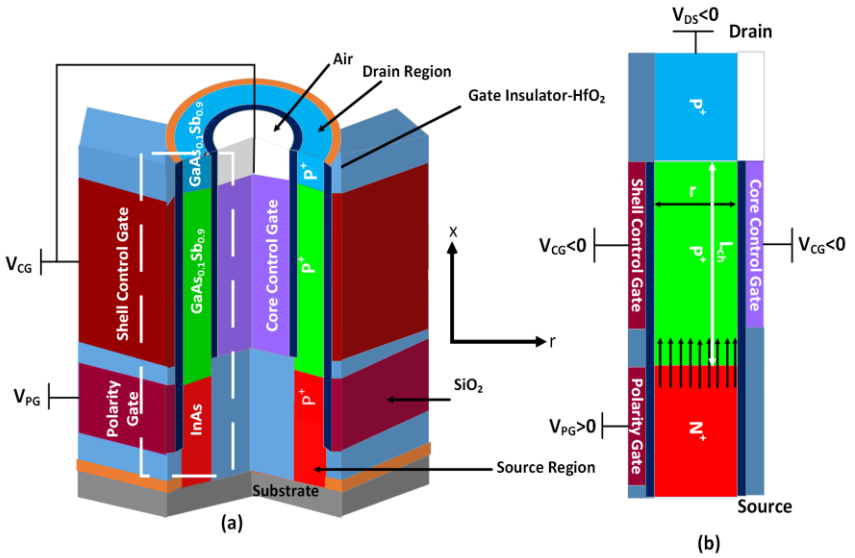

Fig.1: (a) 3D schematic of nanotube core-shell electrically doped heterojunction junctionless TFET with similar doping profile along the device, (b) 2D cross section of the device in the on-state operation in which, due to the positive bias over the source region, the N^+ electron accumulated region is electrically created.

In conclusion, Shockley–Read–Hall (SRH) and trap assisted tunneling models are activated for assessing the effect of carrier transition between localized states. (c) In principle, higher electric fields form biases as well as heavily doped regions strongly influences the carrier mobility. The dependence of the carrier mobility on the horizontal and longitudinal electric field plus its critical effect on the density of dopants and impurities are taking into account via setting proper mobility models. (d) Generally, energy band gap can effectively modulate the tunneling probability. Basically, this can be attributed to the fact that the presence of dopants in highly doped regions of EDHJTFET modifies the locations and configuration of the valence band and conduction band, which eventually leads to the reduction of band gap. Accordingly, band gap narrowing model is activated for considering this effect on the tunneling rate. (e) Generally, quantum confinement reduces the available density of states, which modifies the carrier energy distributions and charge density in the tunneling area. Accordingly, quantum models are adjusted for assessing the device performance as the channel nanotube diameter scales below 5nm. The device follows the fabrication process of vertical nanowire structures. First, rapid

thermal oxidation method is employed for the SiO2 as the insulator region, Next, atomic-layer deposition is used to form core-gate metal gate region and HfO_2 as the gate insulator. the p^+ doped InAs region is formed by molecular beam epitaxy and the $GaAs_{0.1}Sb_{0.9}$ regions are created by atomic layer deposition. Following that, by depositing oxide material and creating contact regions, metal contacts are formed for the shell gate, polarity gate, source and drain regions.

3. RESULTS AND DISCUSSIONS

Basically, band to band tunneling is the main current component of EDHJTFET. In principle, the step like behavior of the device transfer characteristics with steep subthreshold slope, highly depends upon the gate modulated band bending at the source/channel interface. The transmission probability (T) can be described accurately via employing Wenzel-Kramer-Brillouin (WKB) approximation.

The electron and hole density of the proposed EDHJTFET are calculated in the off-state (V_{CG}=0V, V_{PG}=+1V, V_{DS}=-1V) and on-state (V_{CG}=-1V, V_{PG}=+1V, V_{DS}= -1V) operation along the device from source to drain. The carrier density profiles that are illustrated in Fig.2(a), demonstrate that the initial device with $P^+P^+P^+$ doping profile along the source to drain regions are electrically converted to N-i-P^+ region in the off-state. The electrons in the source region are electrically induced via positive bias of the polarity gate. However, due to the workfunction difference between the control gate and the underlying channel and in the absence of control gate bias, the hole density in the channel is considerably reduced. In the on-state operation as the control gate bias goes beyond a sufficient negative values, holes are accumulated in the channel, forming a P^+-N^+ tunneling junction at the source/channel interface. The staircase-like energy band diagram of the staggered type EDHJTFET is illustrated in Fig.2(b) in the off-state and on-state along the device from source to drain. In principle, in the off-state, the conduction band minima of the source region are not aligned with the valence band maxima of the channel region, which inherently suppresses the tunneling probability. It is clearly observed that by applying adequate negative bias to the control gate, the electric field at the tunneling barrier is fundamentally amplified and leads to low resistivity at the source/channel interface. In the on-state, a conductive channel is created from source to drain as the channel valence band moves up to be eventually equivalent to the source conduction band. Figure 3 illustrates impact of gate workfunction on the channel charge density in the off-state (V_{CG}=0V, V_{PG}=1V). It is worth to be mentioned that the drain bias is considered V_{DS}=-0.05V, for

assessing the sole impact of gate workfunction on the modulation of channel charge density. What is noticeable from the channel hole density is that increasing the gate workfunction value considerably enhances the hole density, which warrants the thinnest possible tunneling barrier at the source/channel interface. In principle, the geometric alignment of the P^+N^+ tunneling junction is fundamentally important for the onset of sharp switching behavior of EDHJTFET, which clarifies essential criterion for the gate material choice. It is found that due to the dominant role of polarity gate bias, the gate workfunction exhibits negligible effect on the electrostatically induced source charge. It is well demonstrated that EDHJTFET exploits the operation principle of conventional TFET and clearly requires a steep P^+-N^+ tunneling junction. The electrically induced electrons in the source region fundamentally depends upon the polarity gate bias and gate workfunction values, which needs to be tuned precisely. To analyze the relative sensitivity of each parameter on the density of electrically induced carriers in the source region, the electron density is calculated along the source region as the polarity gate workfunction is varied for different polarity gate biases, illustrated in Fig.4. The results are calculated in the off-state for (V_{CG}=0V, V_{DS}=-0.05V). It is observed that for low values of polarity gate bias, the carrier density is highly contingent on the workfunction difference between the source and the gate material. However, as the polarity gate increases beyond a sufficient value, the electron density is insensitive to the gate workfunction variation, which manifests the proper combination of polarity gate and workfunction values for achieving steep tunneling junction.

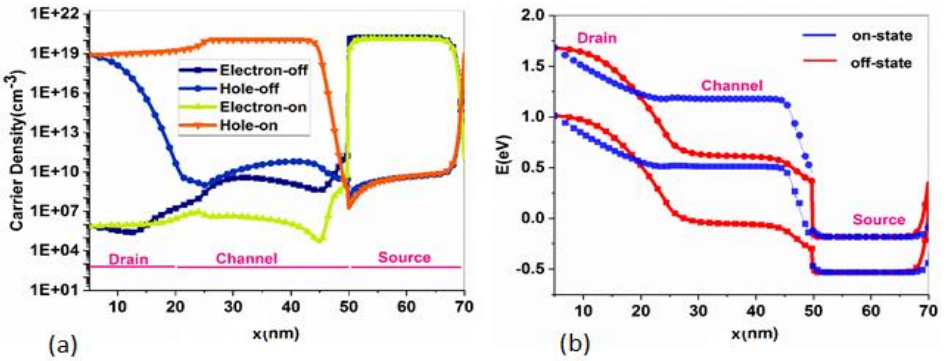

Fig.2: (a) Electron and hole density (b) conduction and valence band energy profile along the device from source to drain in the off-state and on-state operation.

The transfer characteristics of the device is presented in Fig. 5(a) as the drain voltage is parametrized. The device exhibits a step like behavior from the off-state to the maximum on-state current with steep subthreshold slope. In

principle, with the increment of drain bias the average hole velocity in the channel enhances, leading to the improvement of on-state current. However, the main feature of the proposed EDHJTFET is the insensitivity of the off-state current and the threshold voltage to the variation of the drain bias, which confirms the feasibility of the device in nanoscale regime. The results demonstrate that for V_{DS}=1V, on/off current ratio of 9.41×10^{8} and subthreshold swing of 8.7 mV/dec. Moreover, the output characteristics of the EDHJTFET is illustrated in Fig. 5(b) as the gate voltage is varied. The results demonstrate that the control gate voltage variation has a considerable effect on the drain current and as the control gate bias exceeds beyond the threshold voltage, a considerable increment of on-state current is observed. In addition, the device output characteristics represent acceptable saturation behavior with low channel resistance.

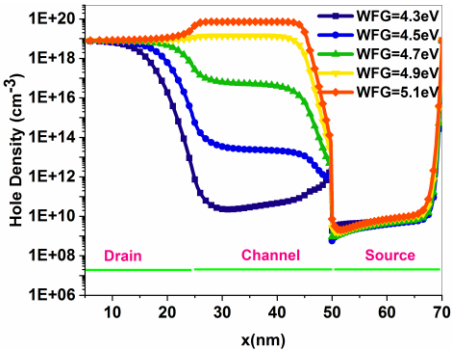

Fig.3: Hole density along the device from source to drain for V_{CG}=0V, V_{PG}=1V and V_{DS}=-0.05V as the workfunction of control gate and polarity gate are parametrized.

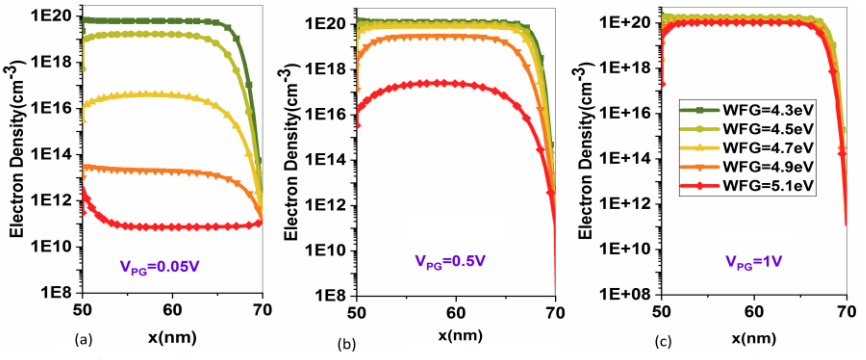

Fig.4: Electron density along the source region for V_{CG}=0Vand V_{DS}=-0.05V as the workfunction and bias of the polarity gate are parametrized.

Figure.6 illustrates the transfer characteristics of EDHJTFET as the temperature (T) is parametrized. It can be observed that due to the dominant role of band to band tunneling current, the on-state current is rarely susceptible to the variation of the temperature. However, the off-state current that is mainly attributed to the source minority carriers, faces a considerable variation and as the temperature rises, the enhancement in the leakage current is expected. The effect of control gate workfunction on the transfer characteristics of the device is illustrated in Fig.7(a). Due to the symmetric metal gate workfunction value over the source and channel regions, a great dependency of tunneling rate to the gate material is expected. Clearly, reduced value of gate workfunction makes lower induced concentration of holes in the channel that will shift the channel Fermi level above the valence band. The results demonstrate that as the gate workfunction is reduced, the transition voltage shifts towards higher negative values, which manifests the employment of reasonable optimum value for the gate material. Clearly, the work function difference between channel material and gate electrodes should be high enough to ensure a low negative voltage for the onset of tunneling. The effect of doping density on the on-state current (Ion) and threshold voltage of the device is comprehensively investigated, depicted in Fig.7(b). In principle, due to the absence of any doping density gradient along the device, the optimum doping density that is required to achieve satisfying high drive current should be precisely assessed. The results demonstrate that as the hole density is enhanced, the tunneling probability that is highly proportional to the tunneling barrier is inherently reduced. Accordingly, the on-state current is increased and the transition voltage shifts towards positive values.

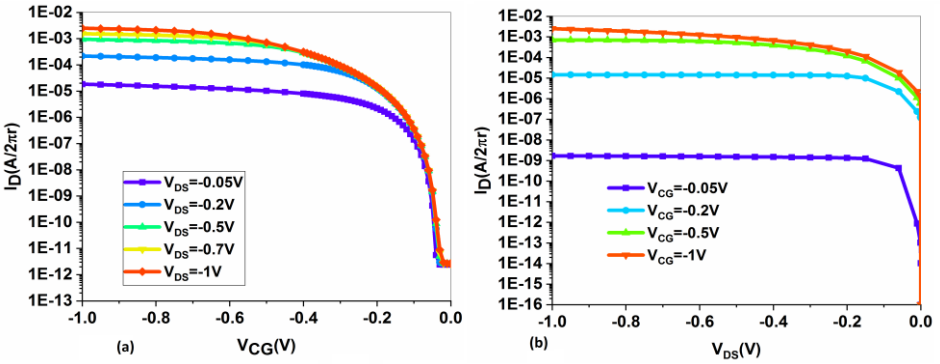

Fig.5: (a) Transfer characteristics of the EDHJTFET as the drain voltage is parametrized. (b) The I_D-V_{DS} profile of the EDHJTFET as the control gate voltage is varied.

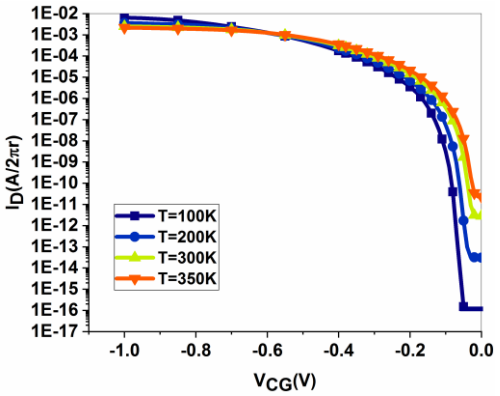

Fig.6: Transfer characteristics of the EDHJTFET as the temperature is varied.

The transconductance and frequency response of the device is illustrated in Fig.8(a). The results demonstrate that cut-off frequency of 200GHz has been achieved, which manifests the feasibility of the device for high frequency application. The bar chart that is illustrated in Fig.8(b), demonstrates the susceptibility of fundamental electrical parameters with respect to the variation of important geometrical parameters. The sensitivity is defined as the standard deviation over mean value in percentile and is calculated for each electrical measures. The results demonstrate that gate workfunction and doping density are critical design parameters that may affect the charge density at the tunneling junction, which requires to be optimized. The insensitivity of off-state current and threshold voltage to the variation of channel length and drain voltage, facilitates the application of the device in nanoscale regime.

4. CONCLUSION

In conclusion, the proposed EDHJTFET provides superior improvement in the on-state current, subthreshold swing and high frequency performance. The polarity gate bias as well as polarity gate workfunction are fundamental parameters that may affect the density of electrically induced charges in the source region, which requires to be optimized. Moreover, the sensitivity analysis reveals that control gate workfunction and doping density can effectively modulate the voltage for the onset of tunneling, which needs to be tuned accurately. The insensitivity of subthreshold swing and off-state current to the variation of channel length and drain voltage manifests the employment of this device in nanoscale regime.

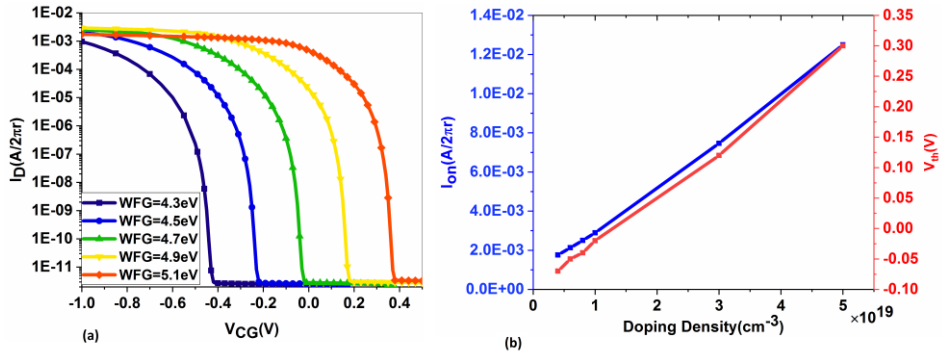

Fig.7: (a) Transfer characteristics of EDHJTFET as a function of gate workfunction. (b) On-state current and threshold voltage of the device versus doping density.

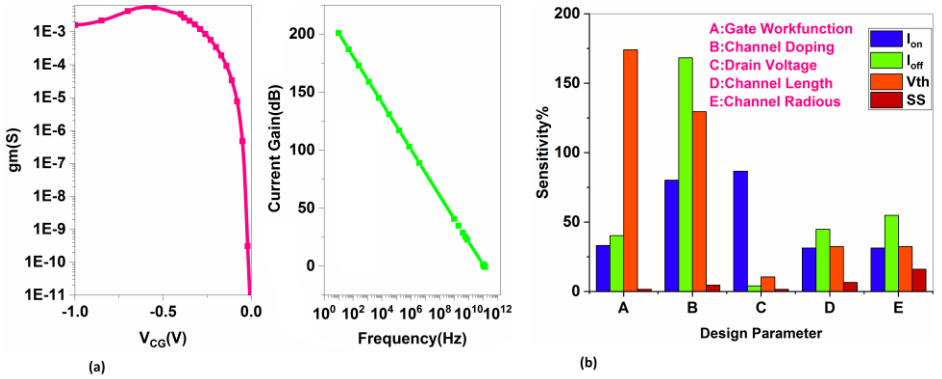

Fig.8: (a) Transconductance versus control gate voltage and frequency response of EDHJTFET (b) Sensitivity bar chart of main design parameters.

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